

LCFC Confidential


YOGA3-BDW M/B Schematics Document

INTEL Broadwell Mobile ULT Platform
INTEL BDW U-series CPU + DDR3L DIMM+ NV N16S-GT

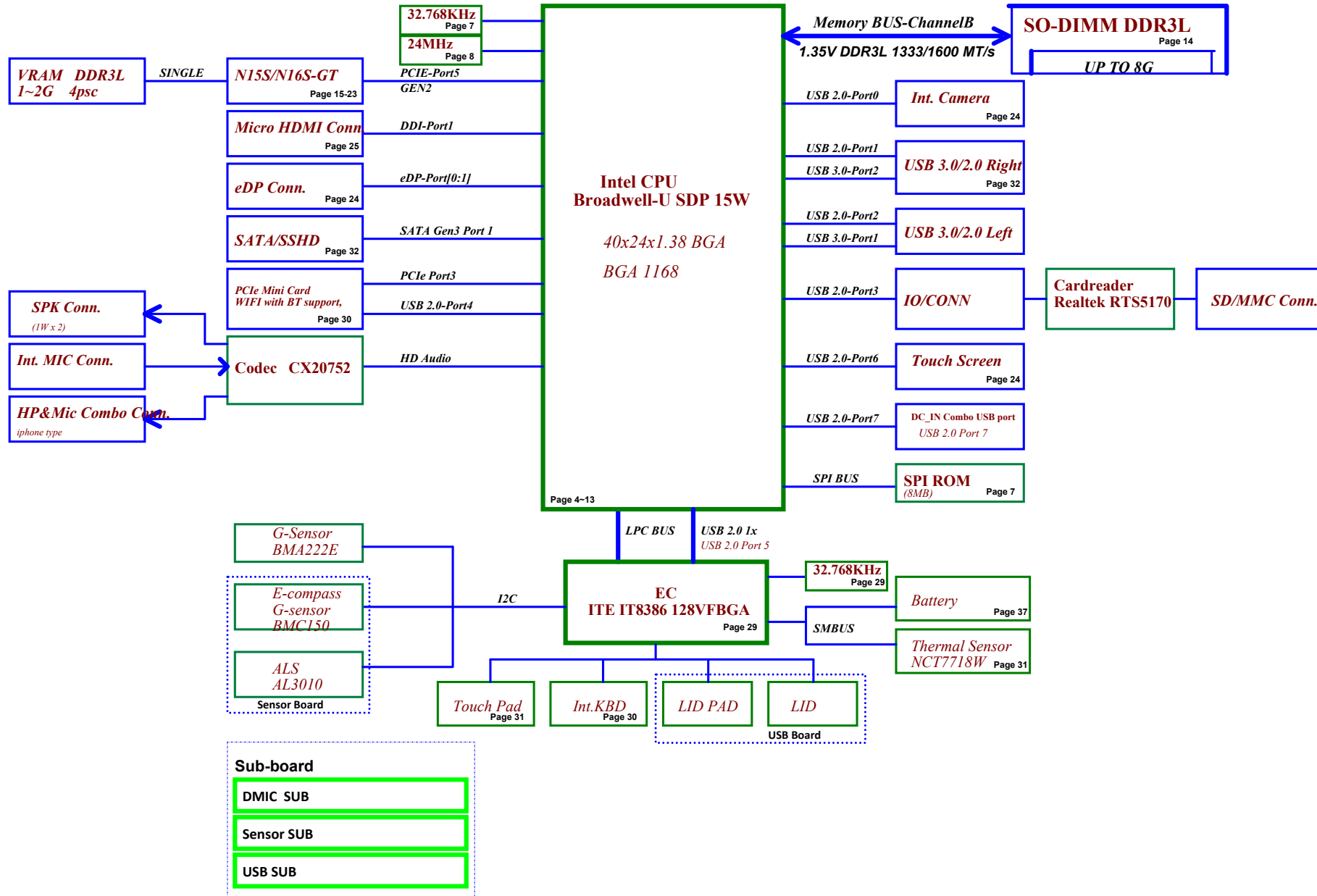
2014-04-28

REV:1.0

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2014/01/11	Deciphered Date	2013/11/08	Cover Page	
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Yoga3 BDW Refresh Block diagram



Power Plane State	B+ +3VL +5VLP	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS +CPU_CORE	+1.35V_CPU
S0	O	O	O	O	O	O
S3	O	O	O	O	X	O
DS3	O	O	X	O	X	X
S5 S4/AC Only	O	O	O	X	X	X
S5 S4 Battery only	O	X	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X	X

SMBUS Control Table

SM Bus address

PCIE PORT LIST










USB Port Table

	USB20	USB30
0	CAMERA	1 Left USB
1	Right USB	2 Right USB
2	Left USB	3 X
3	CARD READER	4 X
4	BT	
5	Sensor	
6	TOUCH PANEL	
7	DC_IN combo USB2.0	

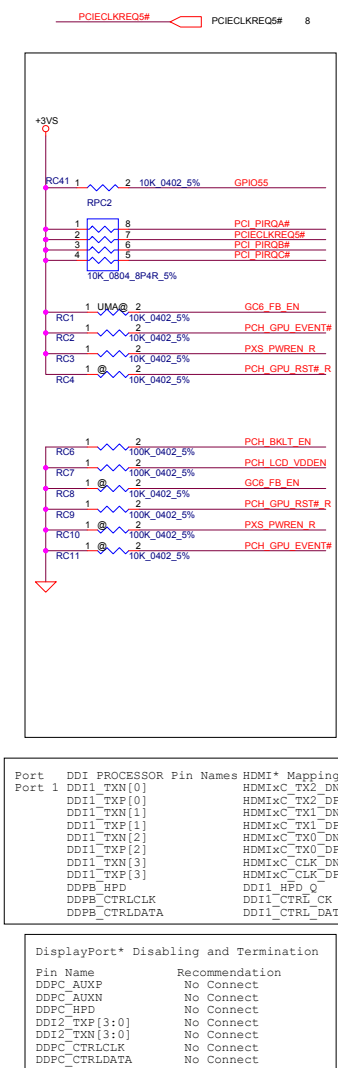
BOM Structure		BOM Structure	
DAB@	PCB	MIRROR@	EC Mirror-code enable
UMA@	UMA SKU part	UNMIRROR@	EC Mirror-code disable
DEBUG@	DEBUG CARD Part	OPT@	Discrete GPU SKU part
ME@	ME part(connector, hole)	N15SGT@	For N15S-GT GPU part
RF@	RF request	GC6@	GC62.0 support part
EMC@	EMC request	RANKA@	For VRAM RankA part
CD@	COST DOWN Part		
REV@	RESERVER Part		


X76&VGA Configuration Table

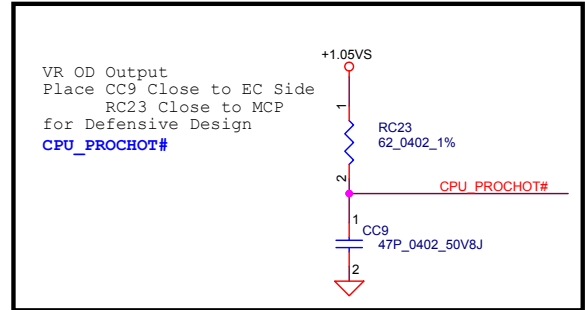
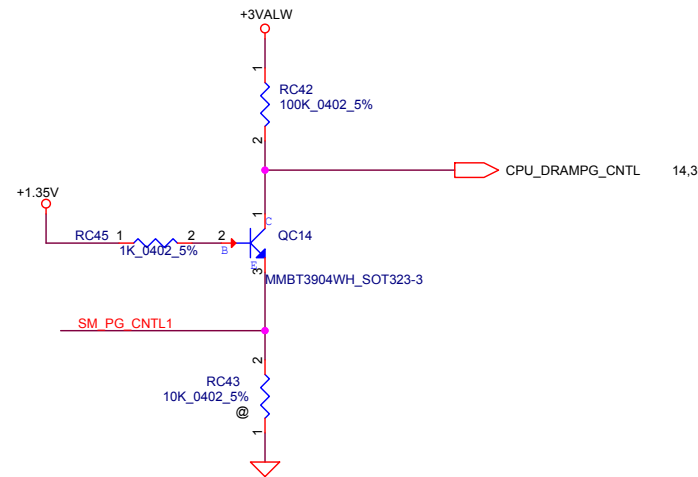
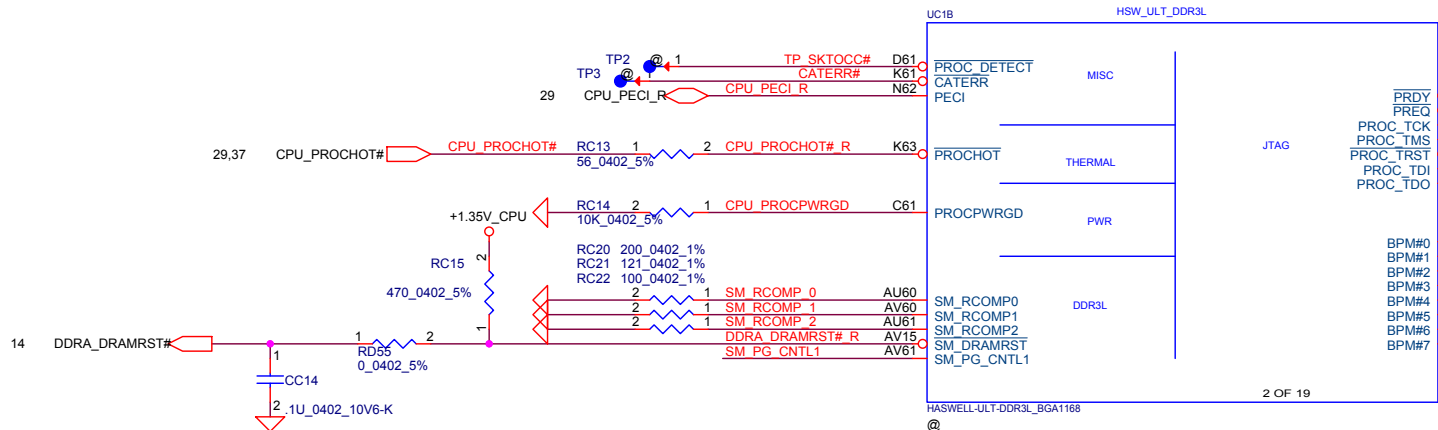
PCB And LOGO Config

PCB	 <p>PCB 0YC NM-A381 REV0 M/B</p>	 
CPU	   <p>BDW U2+2 C17 BDW U2+2 C15 BDW 2+2U 1.6G 1333 ES2</p>	
VRAM	   <p>HYNIX 2G MICRON 2G SAMSUNG 2G</p>	



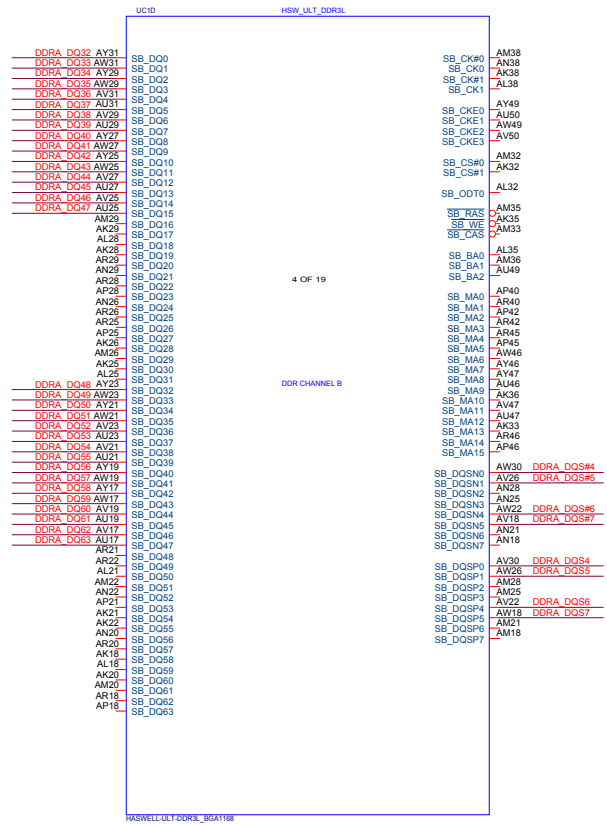
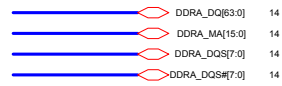
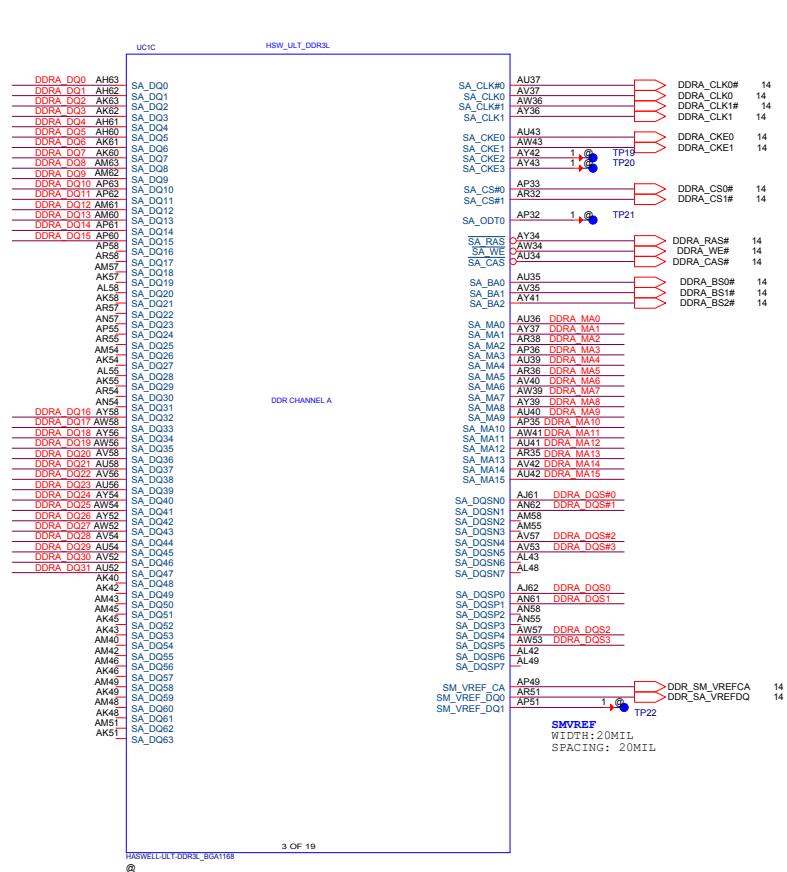


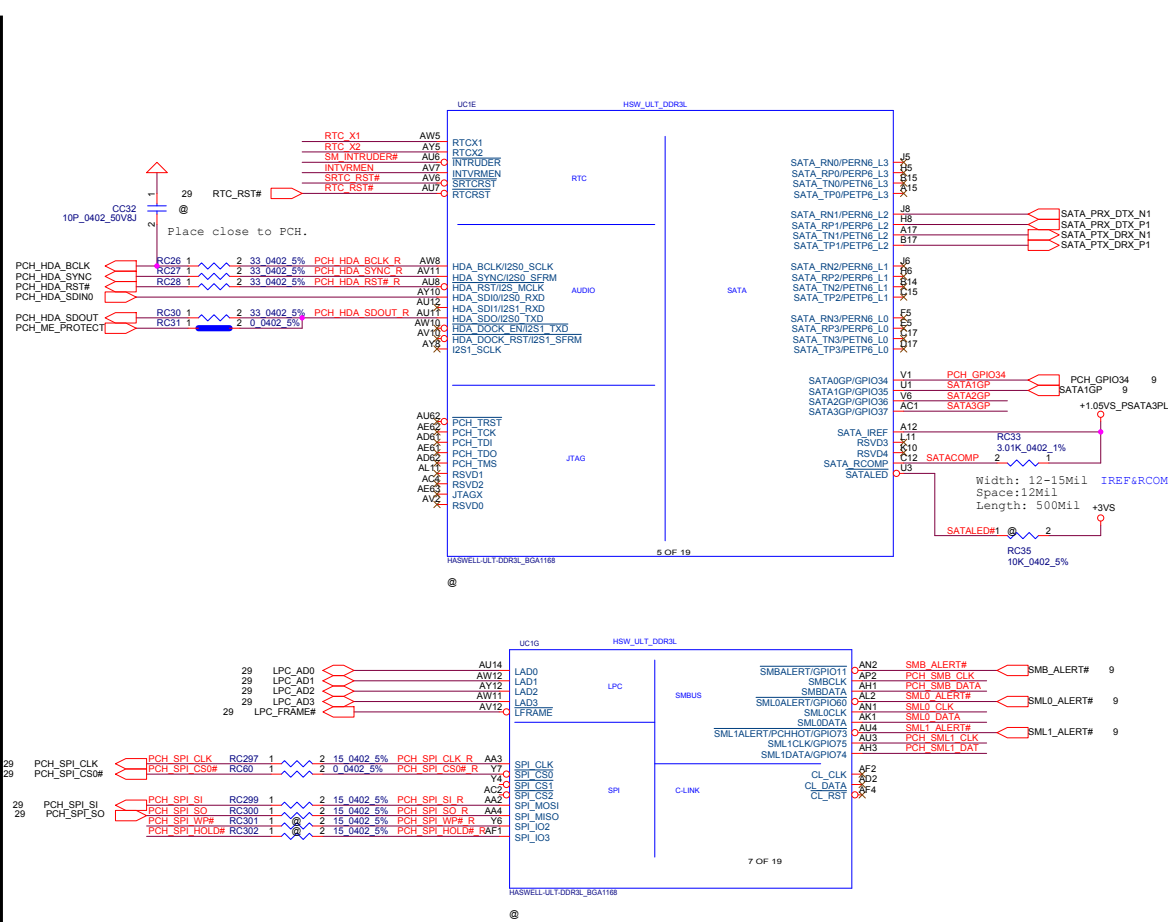
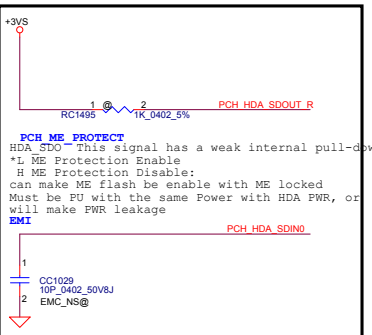
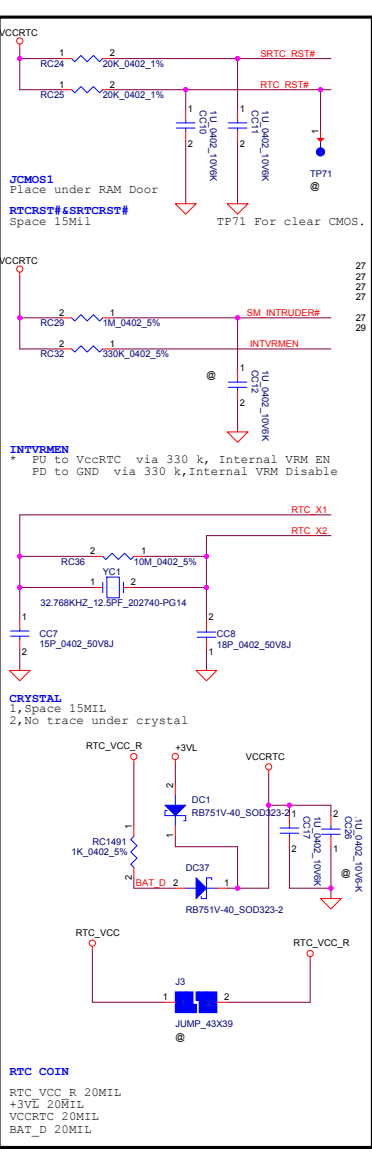
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Issued Date		Deciphered Date		MCP (DDI,EDP)			
2014/01/11		2013/11/08		Size C Document Number Haydn Ray		Date: Monday, November 17, 2014 Sheet 4 of 45	



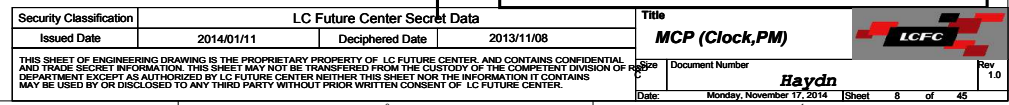
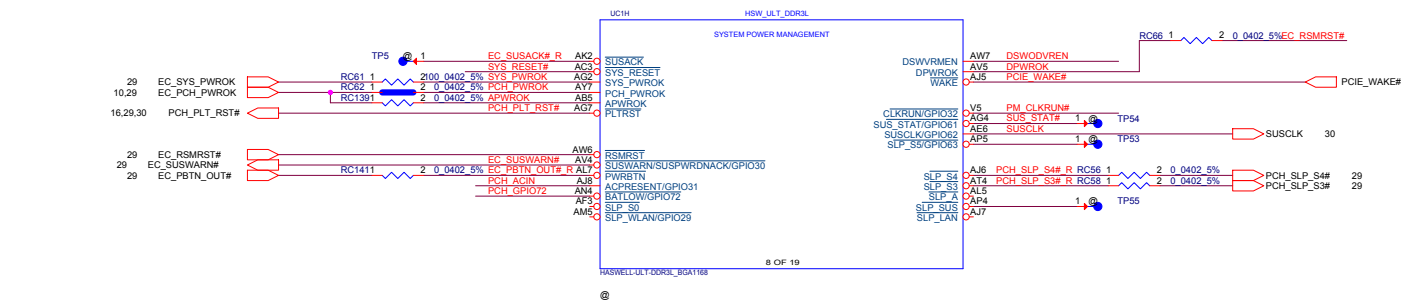
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Issued Date	2014/01/11	Deciphered Date	2013/11/08	MCP (MISC,THERMAL,JATG)	
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				Rev	1.0

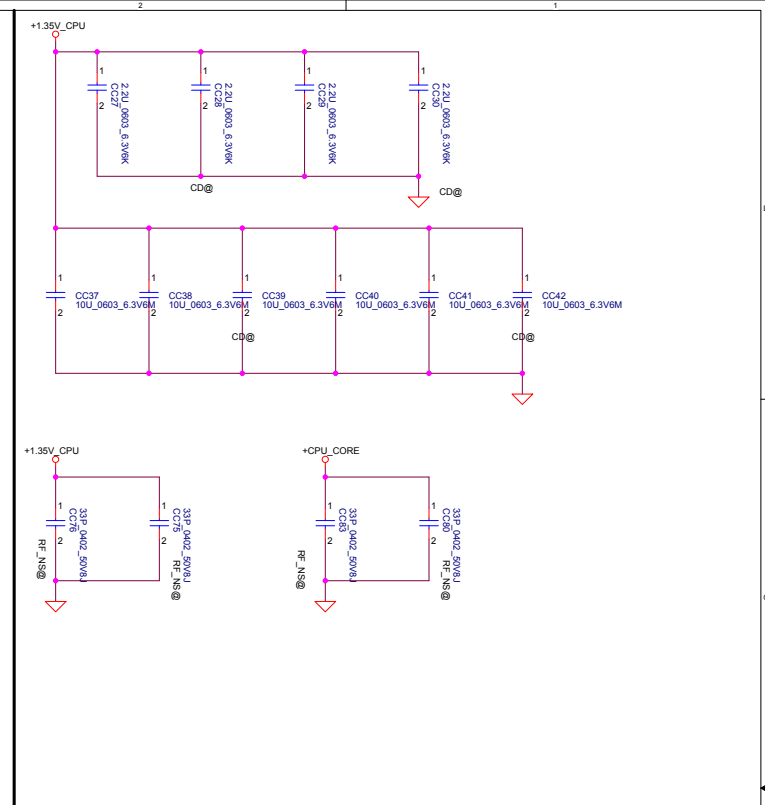
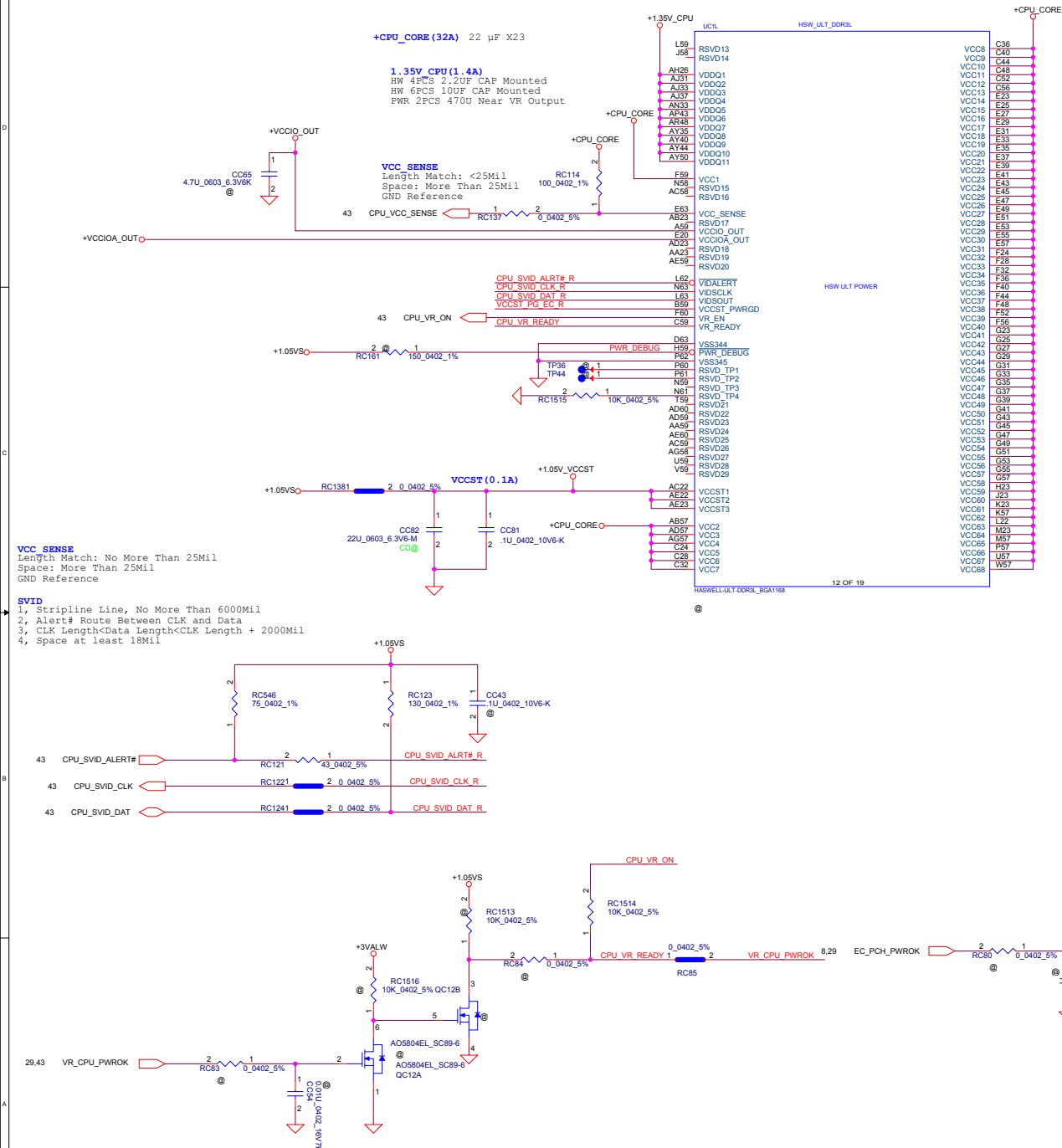
BDW-U 使用so-dimm时,白皮书给出的参照依据是interleaved,





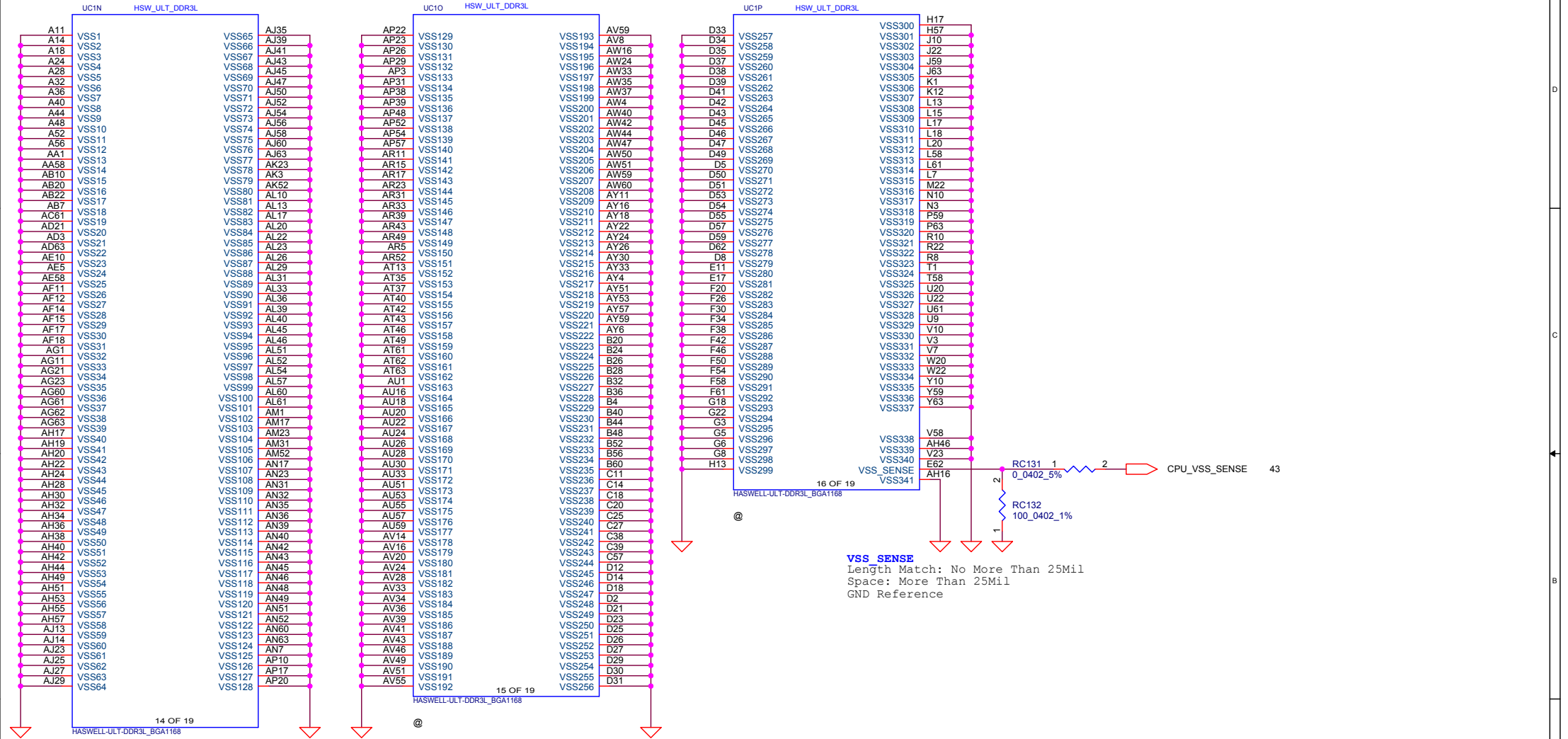
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[illegible]

Haswell MCP (VSS)



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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

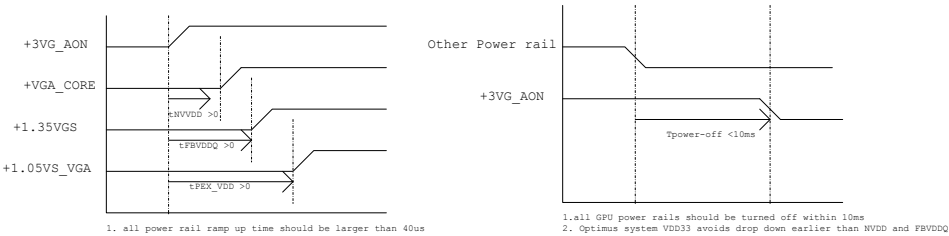
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (s)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

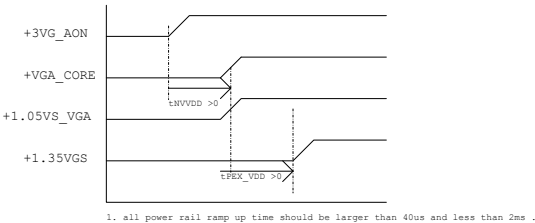
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3 EXPOSED	SOR2 EXPOSED	SOR1 EXPOSED	SOR0 EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



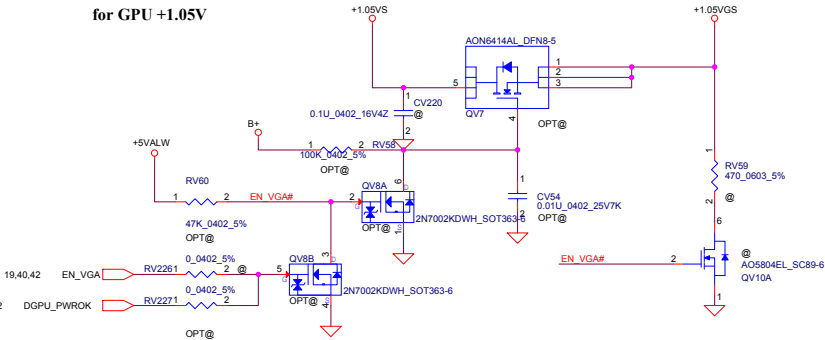
N15S-GT Power Sequence



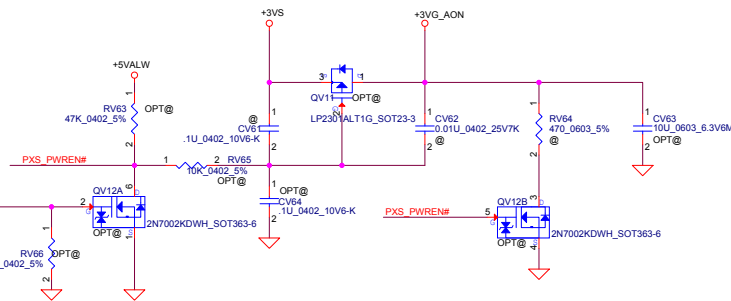
N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

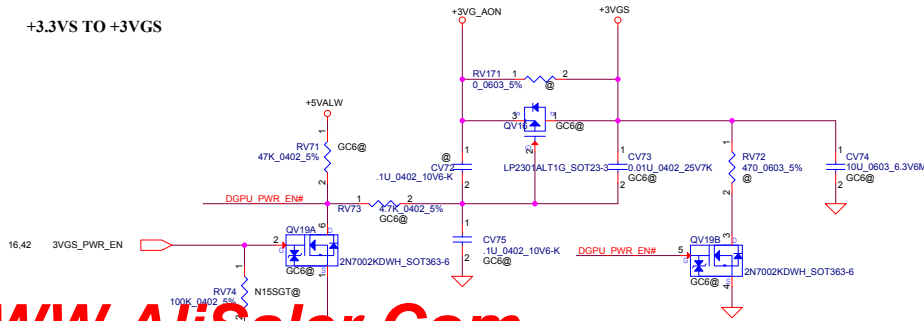
for GPU +1.05V



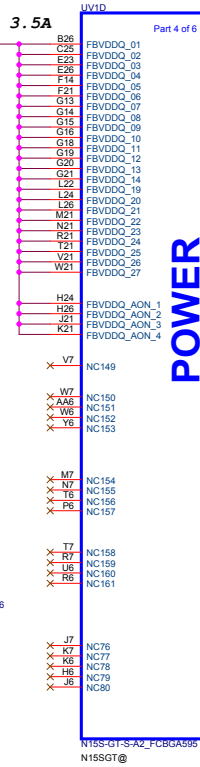
+3.3VS TO +3VG_AON



+3.3VS TO +3VGS



POWER



2000mA

Part 4 of 6

PEX_I0VDD_01

PEX_I0VDD_02

PEX_I0VDD_03

PEX_I0VDD_04

PEX_I0VDD_05

PEX_I0VDD_06

PEX_I0VDD_07

PEX_I0VDD_08

PEX_I0VDD_09

PEX_I0VDD_10

PEX_I0VDD_11

PEX_I0VDD_12

PEX_I0VDD_13

PEX_I0VDD_14

PEX_I0VDD_15

PEX_I0VDD_16

PEX_I0VDD_17

PEX_I0VDD_18

PEX_I0VDD_19

PEX_I0VDD_20

PEX_I0VDD_21

PEX_I0VDD_22

PEX_I0VDD_23

PEX_I0VDD_24

PEX_I0VDD_25

PEX_I0VDD_26

PEX_I0VDD_27

PEX_I0VDD_28

PEX_I0VDD_29

PEX_I0VDD_30

PEX_I0VDD_31

PEX_I0VDD_32

PEX_I0VDD_33

PEX_I0VDD_34

PEX_I0VDD_35

PEX_I0VDD_36

PEX_I0VDD_37

PEX_I0VDD_38

PEX_I0VDD_39

PEX_I0VDD_40

PEX_I0VDD_41

PEX_I0VDD_42

PEX_I0VDD_43

PEX_I0VDD_44

PEX_I0VDD_45

PEX_I0VDD_46

PEX_I0VDD_47

PEX_I0VDD_48

PEX_I0VDD_49

PEX_I0VDD_50

PEX_I0VDD_51

PEX_I0VDD_52

PEX_I0VDD_53

PEX_I0VDD_54

PEX_I0VDD_55

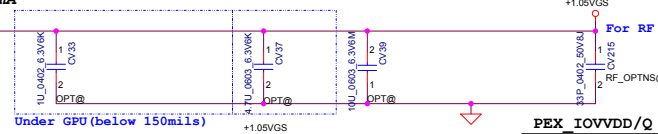
PEX_I0VDD_56

PEX_I0VDD_57

PEX_I0VDD_58

Near GPU

4.7uFX1, 1uFX1, 22uFX1, 10uFX1

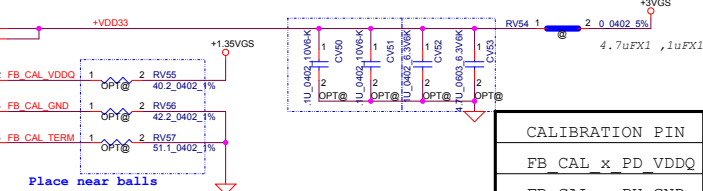


PEX_I0VDD/Q Decoupling

MLCC	N15S-GT	
1.0uF	1	
4.7uF	1	
10uF	1	
22uF	1	

Symbol update to 3V3_AON

Place near balls (Under GPU) Place near GPU



Place near balls

Under GPU (below 150mils)

4.7uFX2, 0.1uFX1

PEX_PLL_VDDQ_1

PEX_PLL_VDDQ_2

PEX_PLL_VDDQ_3

PEX_PLL_VDDQ_4

PEX_PLL_VDDQ_5

PEX_PLL_VDDQ_6

PEX_PLL_VDDQ_7

PEX_PLL_VDDQ_8

PEX_PLL_VDDQ_9

PEX_PLL_VDDQ_10

PEX_PLL_VDDQ_11

PEX_PLL_VDDQ_12

PEX_PLL_VDDQ_13

PEX_PLL_VDDQ_14

PEX_PLL_VDDQ_15

PEX_PLL_VDDQ_16

PEX_PLL_VDDQ_17

PEX_PLL_VDDQ_18

PEX_PLL_VDDQ_19

PEX_PLL_VDDQ_20

PEX_PLL_VDDQ_21

PEX_PLL_VDDQ_22

PEX_PLL_VDDQ_23

PEX_PLL_VDDQ_24

PEX_PLL_VDDQ_25

PEX_PLL_VDDQ_26

PEX_PLL_VDDQ_27

PEX_PLL_VDDQ_28

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PEX_PLL_VDDQ_30

PEX_PLL_VDDQ_31

PEX_PLL_VDDQ_32

PEX_PLL_VDDQ_33

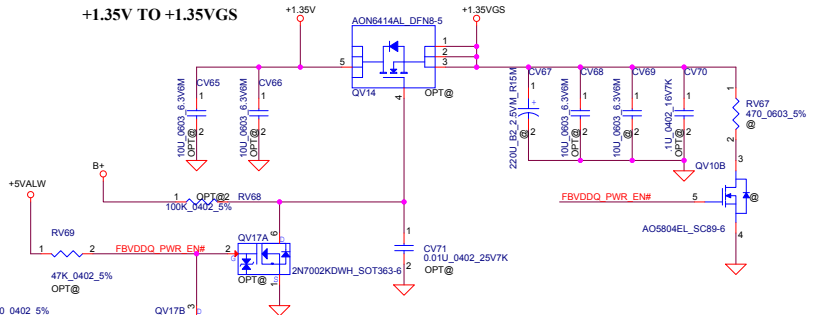
PEX_PLL_VDDQ_34

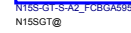
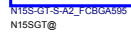
PEX_PLL_VDDQ_35

PEX_PLL_VDDQ_36

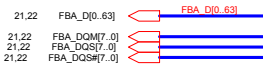
PEX_PLL_VDDQ_37

+1.35V TO +1.35VGS





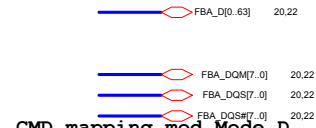
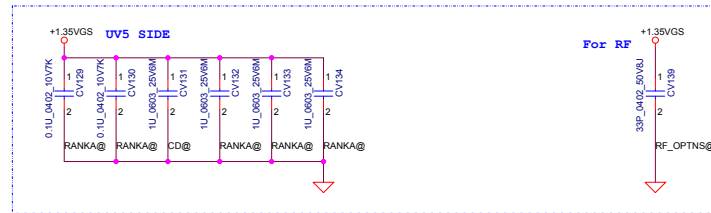
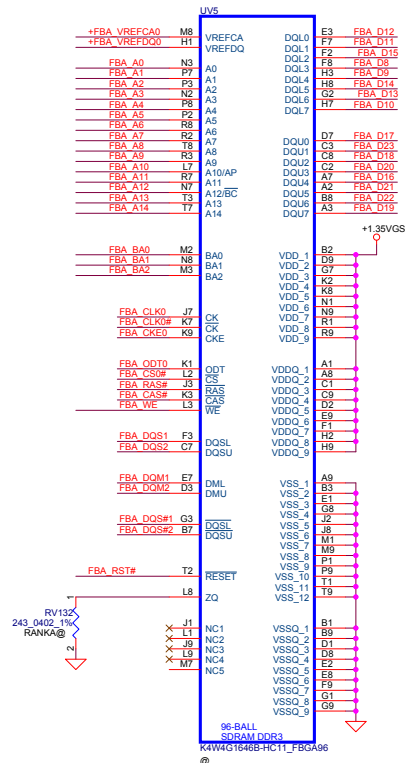
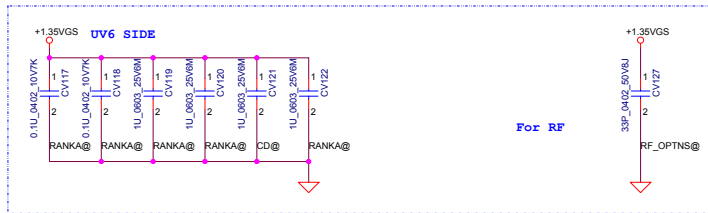
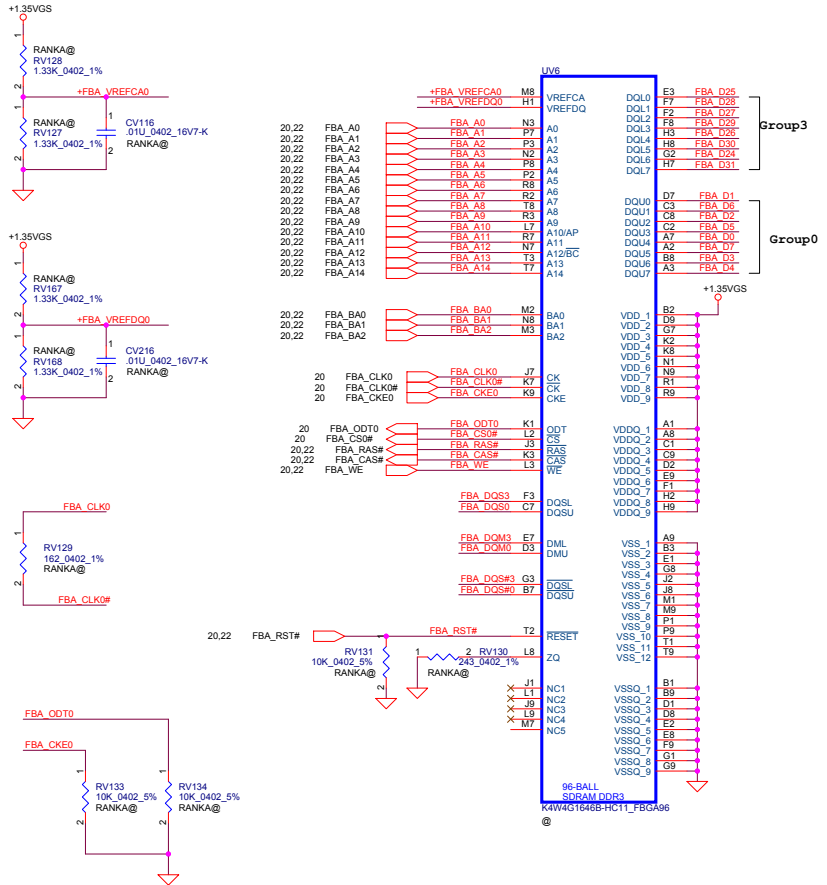
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CMD mapping mod Mode D

Rank0			
Address	0..31	32..63	
FBx_CMD0	CS0#		
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16	CSI#		
FBx_CMD17			
FBx_CMD18	ODT1		
FBx_CMD19	CKE1		
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		

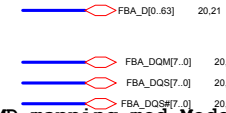
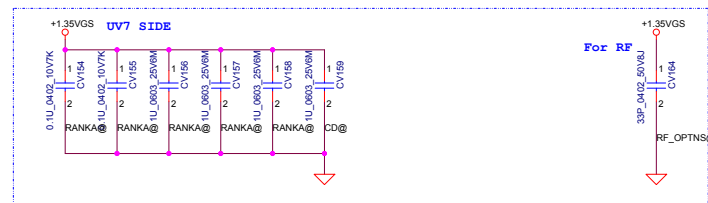
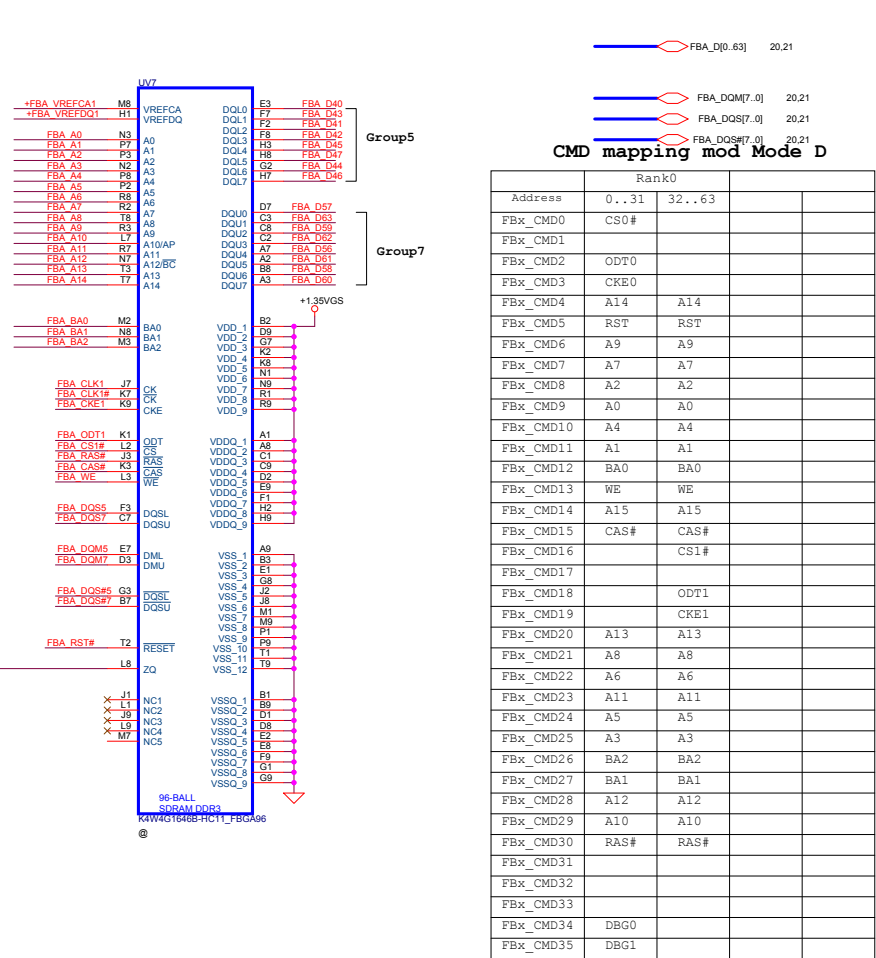
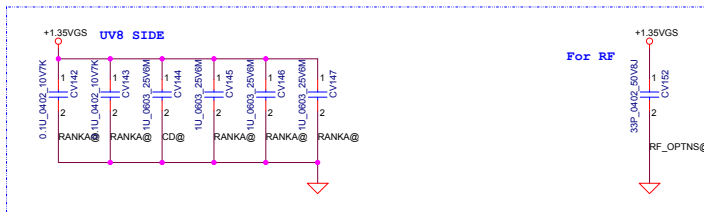
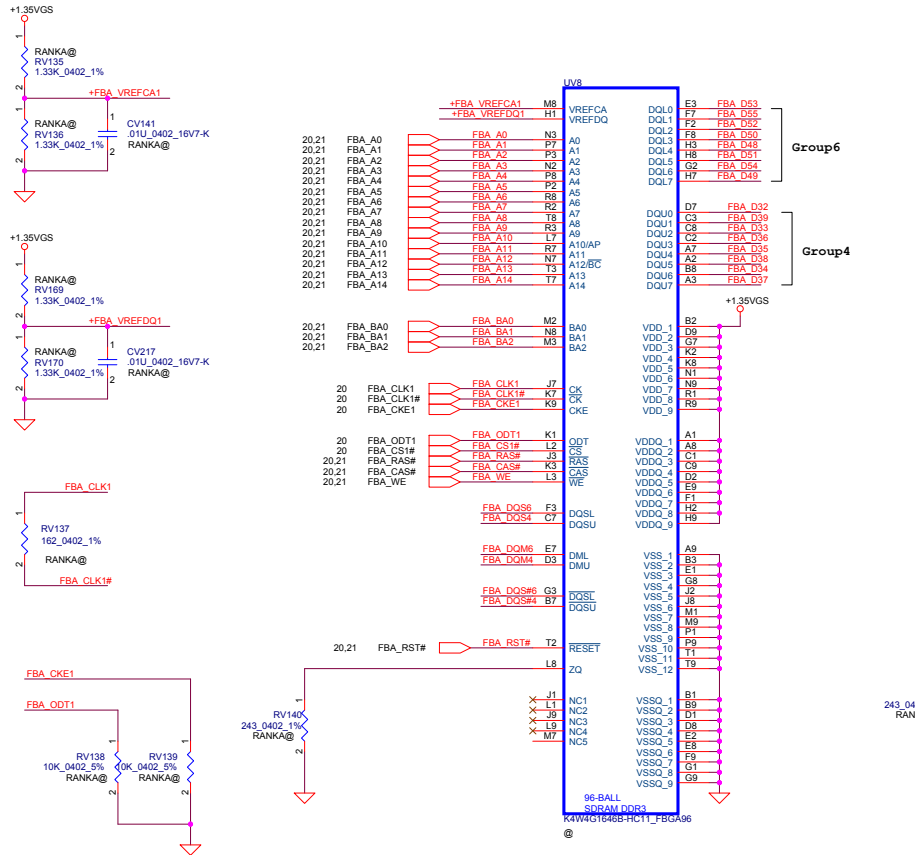
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode D

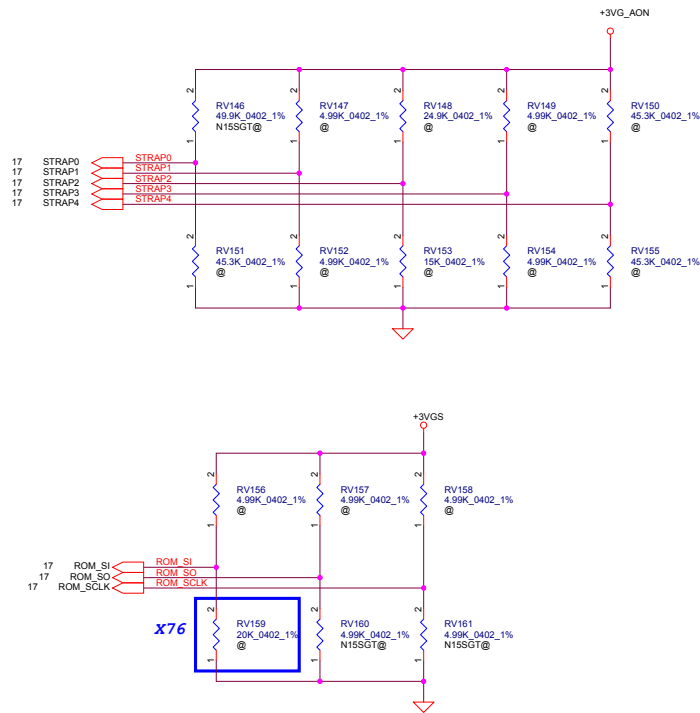
		Rank0	
Address	0..31	32..63	
FbX_CMD0	CS0#		
FbX_CMD1			
FbX_CMD2	ODT0		
FbX_CMD3	CKE0		
FbX_CMD4	A14	A14	
FbX_CMD5	RST	RST	
FbX_CMD6	A9	A9	
FbX_CMD7	A7	A7	
FbX_CMD8	A2	A2	
FbX_CMD9	A0	A0	
FbX_CMD10	A4	A4	
FbX_CMD11	A1	A1	
FbX_CMD12	BA0	BA0	
FbX_CMD13	WE	WE	
FbX_CMD14	A15	A15	
FbX_CMD15	CAS#	CAS#	
FbX_CMD16		CS1#	
FbX_CMD17			
FbX_CMD18		ODT1	
FbX_CMD19		CKE1	
FbX_CMD20	A13	A13	
FbX_CMD21	A8	A8	
FbX_CMD22	A6	A6	
FbX_CMD23	A11	A11	
FbX_CMD24	A5	A5	
FbX_CMD25	A3	A3	
FbX_CMD26	BA2	BA2	
FbX_CMD27	BA1	BA1	
FbX_CMD28	A12	A12	
FbX_CMD29	A10	A10	
FbX_CMD30	RAS#	RAS#	
FbX_CMD31			
FbX_CMD32			
FbX_CMD33			
FbX_CMD34	DBG0		
FbX_CMD35	DBG1		

at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode D

	Rank0	
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT0	
FBx_CMD3	CKE0	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE	WE
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS1#	
FBx_CMD17		
FBx_CMD18	ODT1	
FBx_CMD19	CKE1	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		
FBx_CMD32		
FBx_CMD33		
FBx_CMD34	DBG0	
FBx_CMD35	DBG1	



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

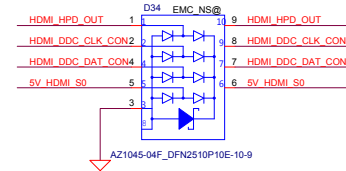
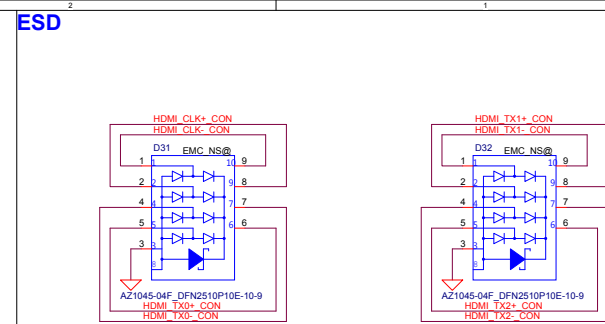
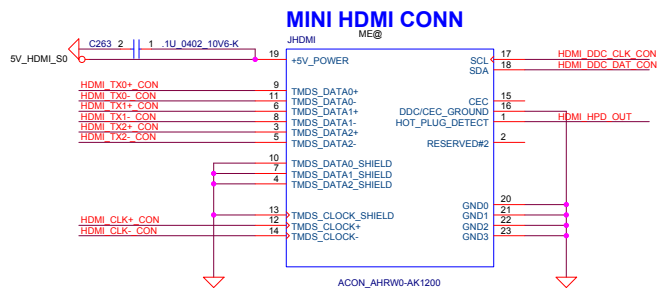
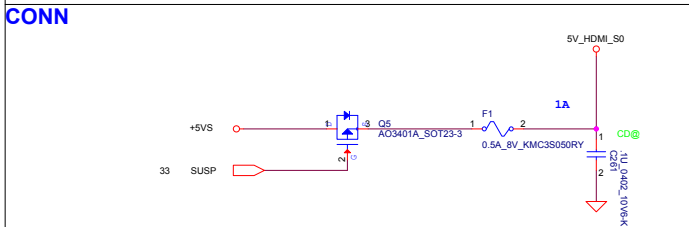
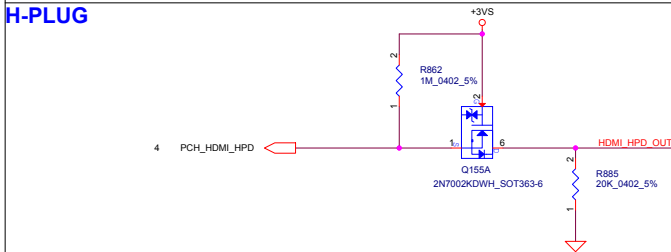
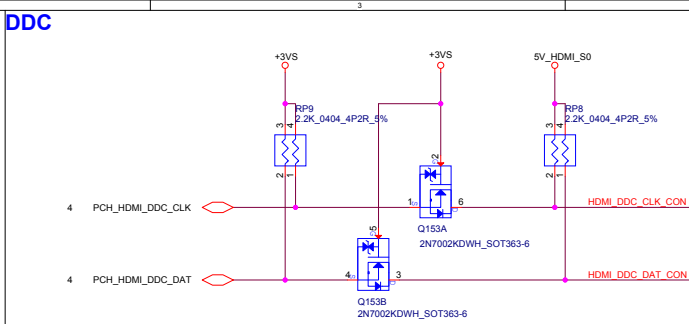
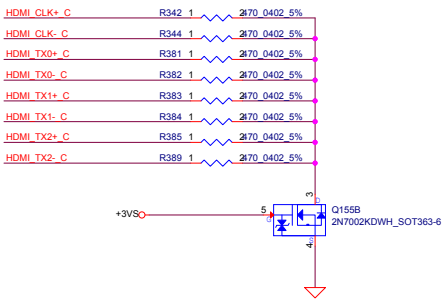
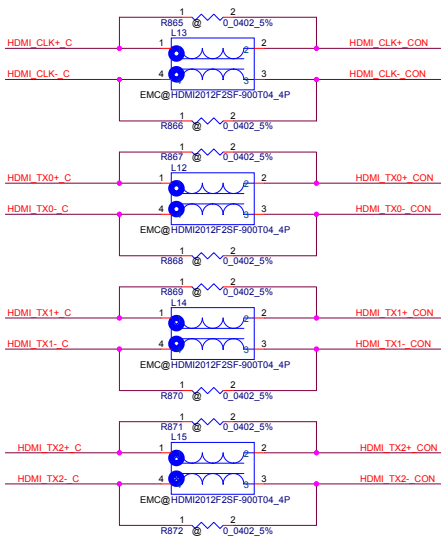
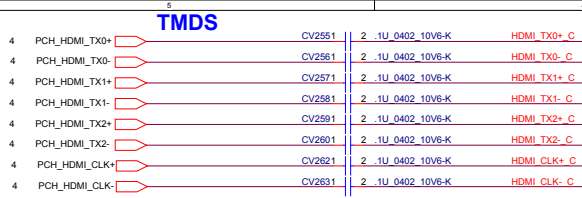
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

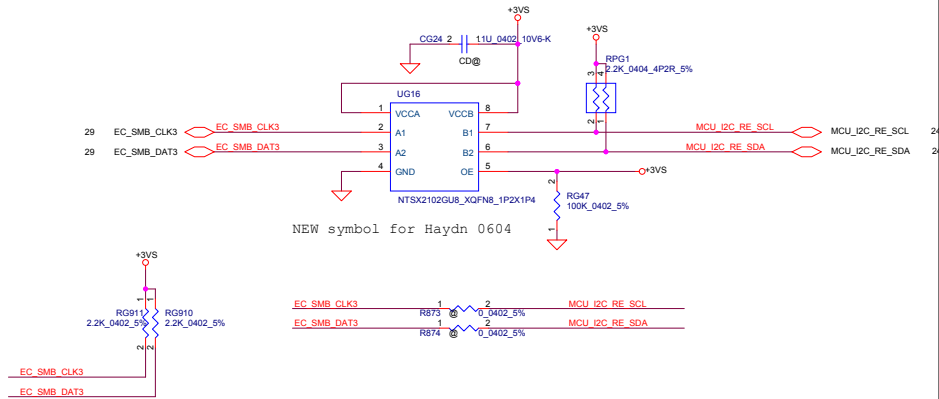
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

N15x Binary Straps		
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

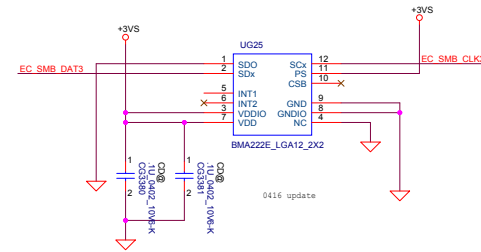
GPU		FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz	H5TC4G63AFR-11C	0x3	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		256M x 16	PD 20K							
	Micron 900MHz	MT41J256M16HA-093G:E	0x4							
		256M x 16	PD 24.9K							
	Samsung 900MHz	K4W4G1646D-BC1A	0x5							
		256M x 16	PD 30.1K							
	Hynix 900MHz	H5TC2G63FFR-11C	0x9							
		128M x 16	PU 10K							
	Micron 900MHz	MT41J128M16JT-093G:K	0xA							
		128M x 16	PU 15K							
	Samsung 900MHz	K4W2G1646Q-BC1A	0xB							
		128M x 16	PU 20K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01	SA00005SH10
	X76409JVL51 (1G 32Mx16)	
Micron	X76409JVL02	SA00005M100
	X76409JVL02 (2G 64Mx32)	
Hynix		





G-SENSOR



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				Haydn	1.0
				Date	Monday, November 11, 2014
				Sheet	26 of 45



JIO HDA CARDREADER USB CONN

RA20
Add for Beep Noise on 5/21

CARD READER
Left USB_CONN

RA28 Close to JIO

NEW symbol for Haydn 0609

For EMI

Security Classification: LC Future Center Secret Data

Issued Date: 2014/01/11

Deciphered Date: 2013/11/08

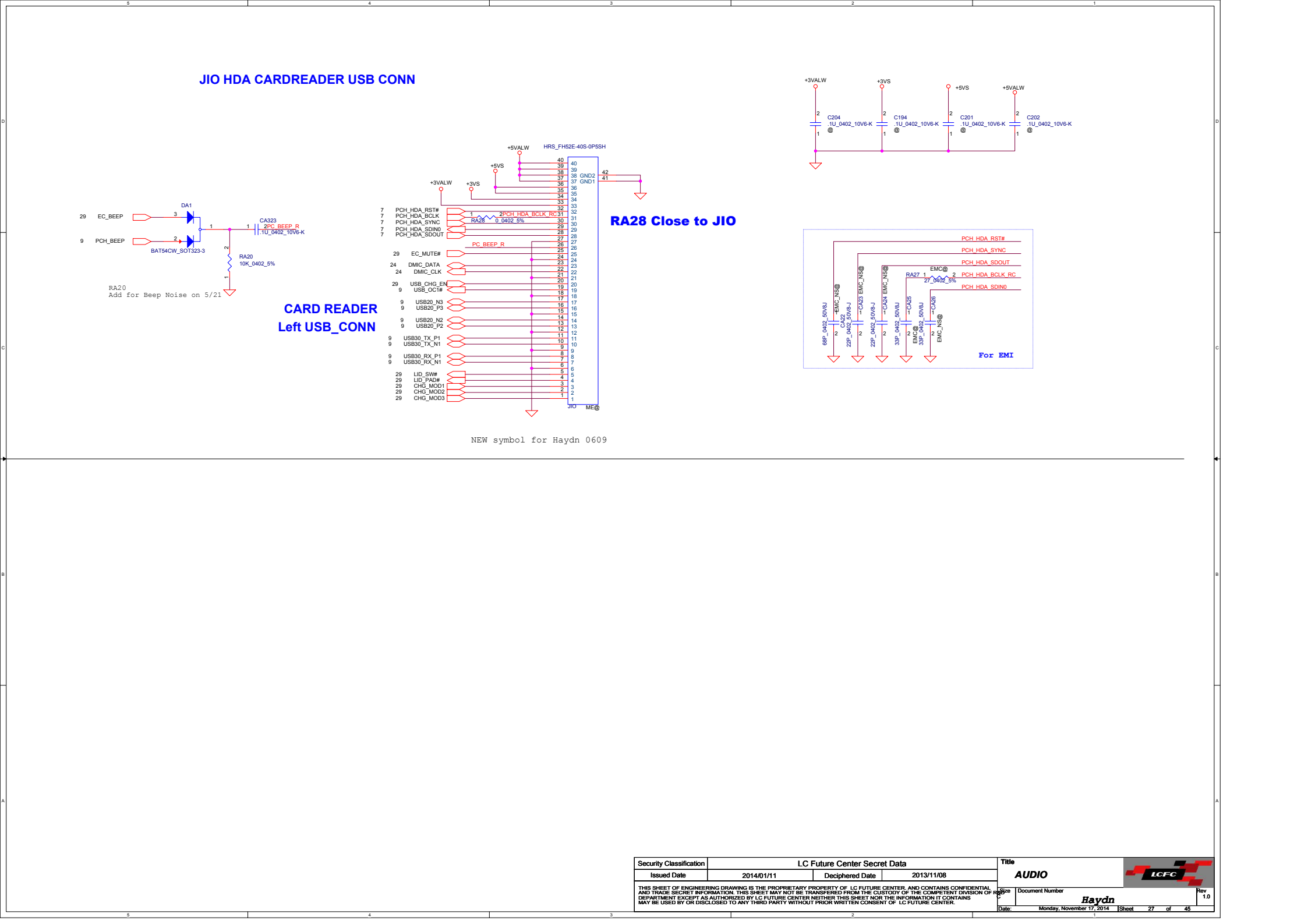
Title: AUDIO

Document Number: Haydn

Date: Monday, November 17, 2014

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JIO HDA CARDREADER USB CONN

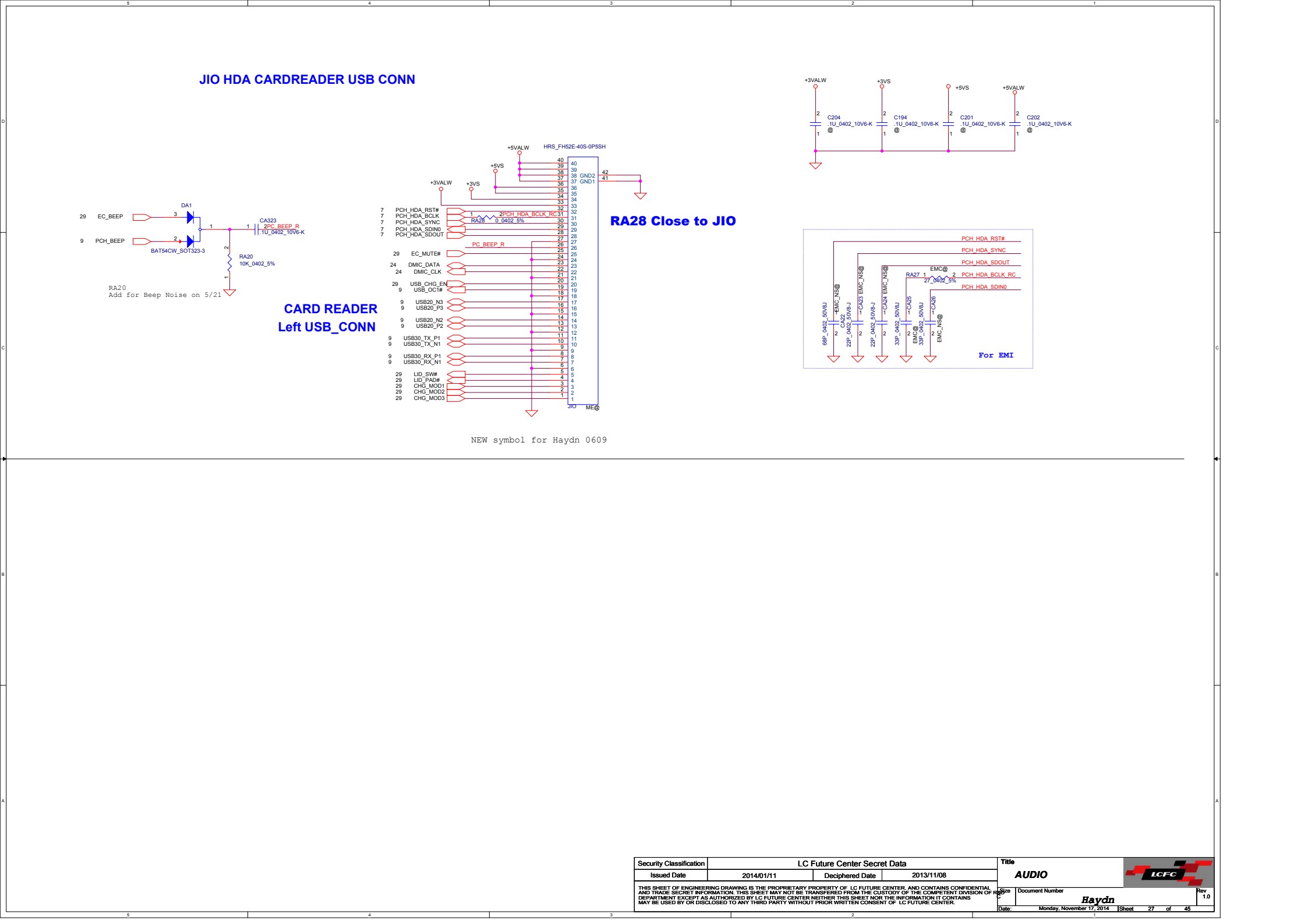
CARD READER Left USB_CONN

RA28 Close to JIO

For EMI

NEW symbol for Haydn 0609

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Issued Date		2014/01/11		Deciphered Date		2013/11/08	
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JIO HDA CARDREADER USB CONN

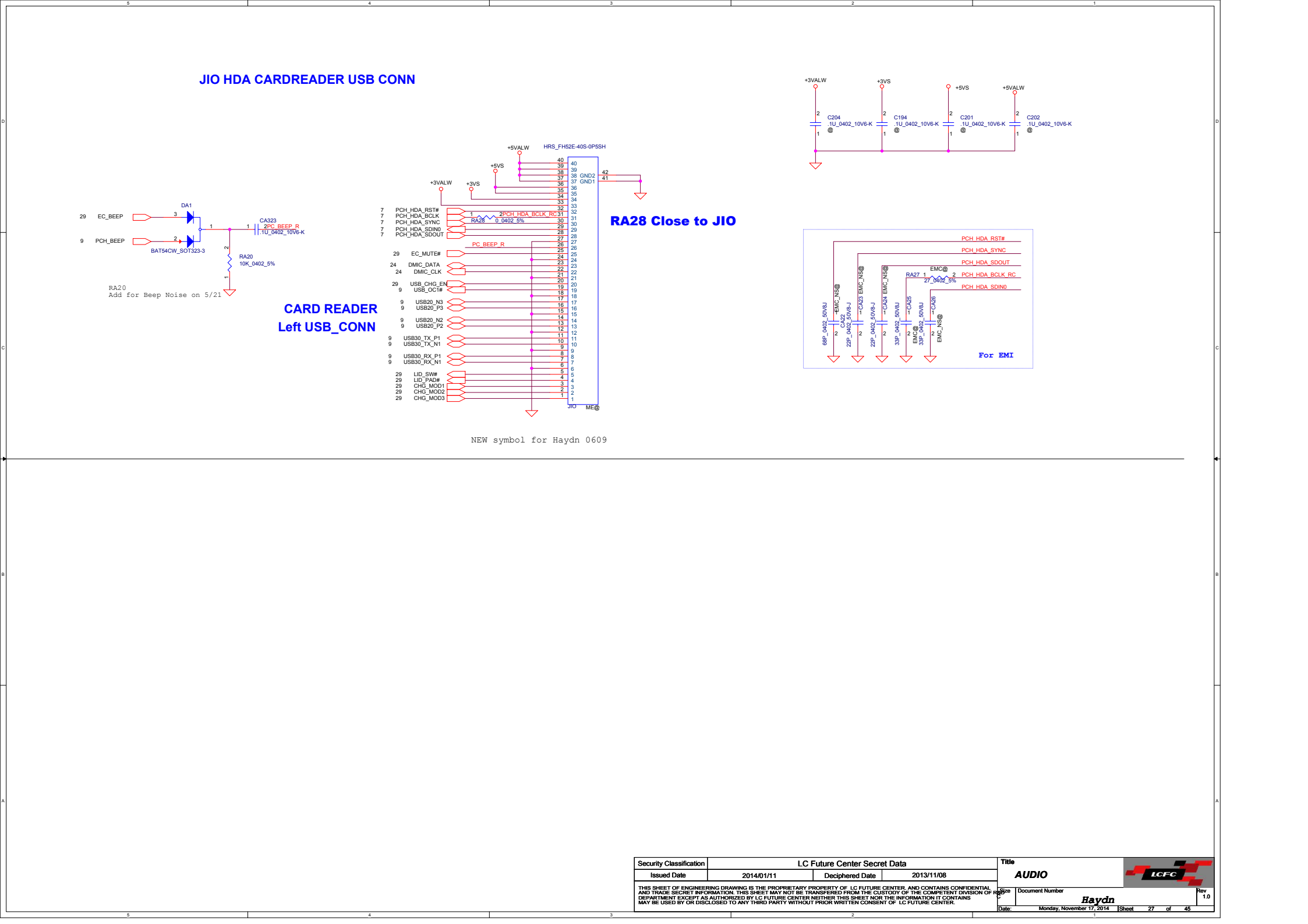
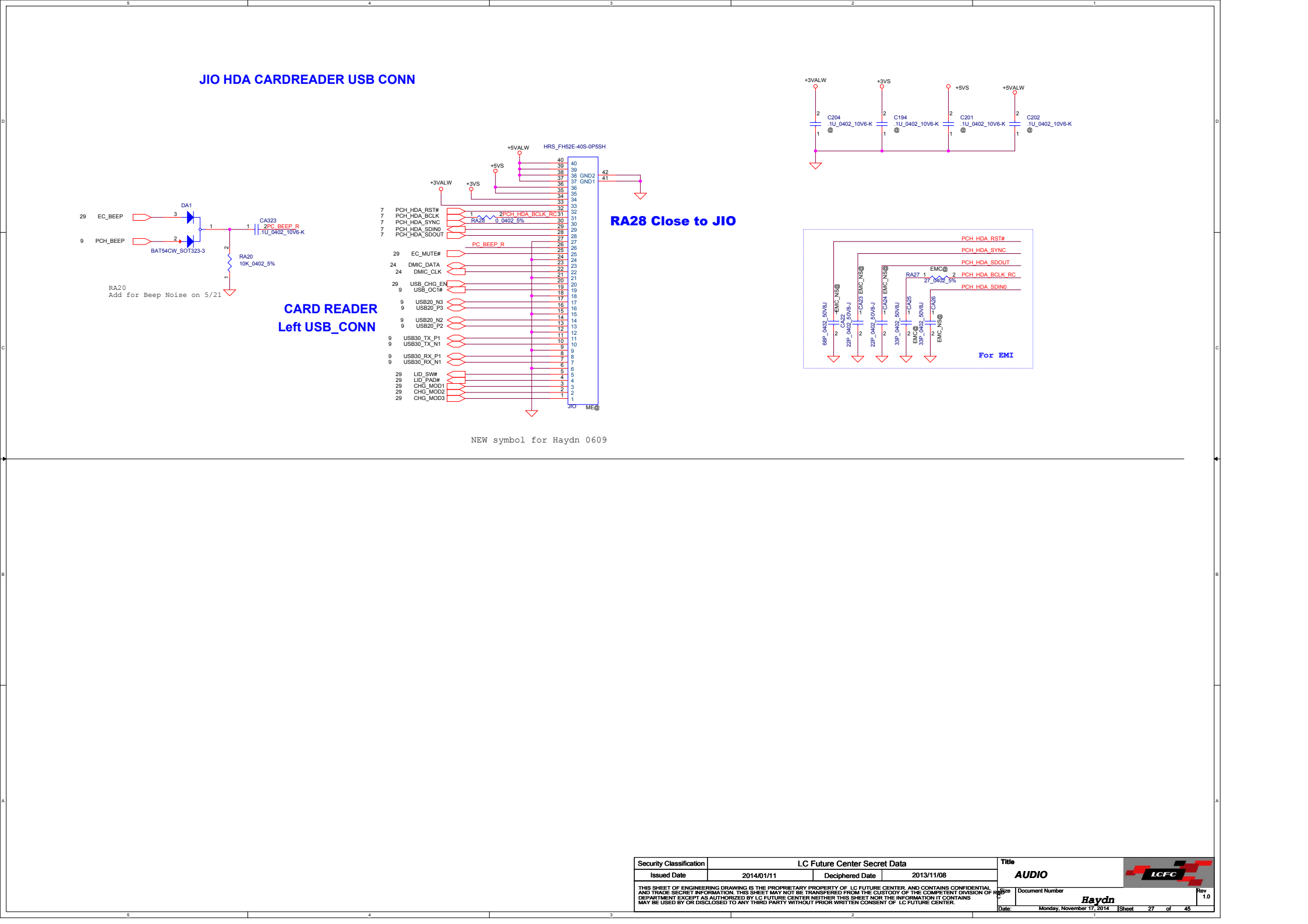
CARD READER Left USB_CONN

RA28 Close to JIO

For EMI

NEW symbol for Haydn 0609

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JIO HDA CARDREADER USB CONN

RA20
Add for Beep Noise on 5/21

CARD READER
Left USB_CONN

RA28 Close to JIO

NEW symbol for Haydn 0609

For EMI

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JIO HDA CARDREADER USB CONN

CARD READER Left USB_CONN

RA28 Close to JIO

For EMI

NEW symbol for Haydn 0609

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
29	EC_BEEP	7	PCH_HDA_RST#	32	PCH_HDA_RST#	40	+5VALW
9	PCH_BEEP	7	PCH_HDA_BCLK	31	PCH_HDA_BCLK	39	+3VS
		7	PCH_HDA_SYNC	30	PCH_HDA_SYNC	38	GND2
		7	PCH_HDA_SDIN0	29	PCH_HDA_SDIN0	37	GND1
		7	PCH_HDA_SDOUT	28	PCH_HDA_SDOUT	36	
				27		35	
				26		34	
				25		33	
29	EC_MUTE#	25	EC_MUTE#	24	DMIC_DATA	23	DMIC_CLK
24	DMIC_DATA	24	DMIC_CLK	23	DMIC_DATA	22	DMIC_CLK
24	DMIC_CLK	23	DMIC_DATA	22	DMIC_CLK	21	DMIC_DATA
29	USB_CHG_EN	20	USB_CHG_EN	19	USB_OCT#	18	USB_OCT#
9	USB_OCT#	18	USB_OCT#	17	USB20_N3	16	USB20_P3
9	USB20_N3	16	USB20_P3	15	USB20_N2	14	USB20_P2
9	USB20_P3	15	USB20_N2	14	USB20_P2	13	USB20_N1
9	USB20_N2	14	USB20_P2	13	USB20_N1	12	USB30_TX_P1
9	USB20_P2	13	USB20_N1	12	USB30_TX_P1	11	USB30_TX_N1
9	USB30_TX_P1	11	USB30_TX_N1	10	USB30_RX_P1	9	USB30_RX_N1
9	USB30_TX_N1	10	USB30_RX_P1	9	USB30_RX_N1	8	USB30_RX_P1
9	USB30_RX_P1	8	USB30_RX_N1	7	LID_SW#	6	LID_PA3#
9	USB30_RX_N1	7	LID_SW#	6	LID_PA3#	5	CHG_MOD1
29	LID_SW#	6	LID_PA3#	5	CHG_MOD1	4	CHG_MOD2
29	LID_PA3#	5	CHG_MOD1	4	CHG_MOD2	3	CHG_MOD3
29	CHG_MOD1	4	CHG_MOD2	3	CHG_MOD3	2	
29	CHG_MOD2	3	CHG_MOD3	2		1	
29	CHG_MOD3	2		1			

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JIO HDA CARDREADER USB CONN

CARD READER Left USB_CONN

RA28 Close to JIO

For EMI

NEW symbol for Haydn 0609

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
29	EC_BEEP	7	PCH_HDA_RST#	32	PCH_HDA_RST#	40	+5VALW
9	PCH_BEEP	7	PCH_HDA_BCLK	31	PCH_HDA_BCLK	39	+3VS
		7	PCH_HDA_SYNC	30	PCH_HDA_SYNC	38	GND2
		7	PCH_HDA_SDIN0	29	PCH_HDA_SDIN0	37	GND1
		7	PCH_HDA_SDOUT	28	PCH_HDA_SDOUT	36	
				27		35	
				26		34	
				25		33	
29	EC_MUTE#	25	EC_MUTE#	24	DMIC_DATA	23	DMIC_CLK
24	DMIC_DATA	24	DMIC_CLK	23	DMIC_DATA	22	DMIC_CLK
24	DMIC_CLK	23	DMIC_DATA	22	DMIC_CLK	21	DMIC_DATA
29	USB_CHG_EN	20	USB_CHG_EN	19	USB_OCT#	18	USB_OCT#
9	USB_OCT#	18	USB_OCT#	17	USB20_N3	16	USB20_P3
9	USB20_N3	16	USB20_P3	15	USB20_N2	14	USB20_P2
9	USB20_P3	15	USB20_N2	14	USB20_P2	13	USB20_N1
9	USB20_N2	14	USB20_P2	13	USB20_N1	12	USB30_TX_P1
9	USB20_P2	13	USB20_N1	12	USB30_TX_P1	11	USB30_TX_N1
9	USB30_TX_P1	11	USB30_TX_N1	10	USB30_RX_P1	9	USB30_RX_N1
9	USB30_TX_N1	10	USB30_RX_P1	9	USB30_RX_N1	8	USB30_RX_P1
9	USB30_RX_P1	8	USB30_RX_N1	7	LID_SW#	6	LID_PA3#
9	USB30_RX_N1	7	LID_SW#	6	LID_PA3#	5	CHG_MOD1
29	LID_SW#	6	LID_PA3#	5	CHG_MOD1	4	CHG_MOD2
29	LID_PA3#	5	CHG_MOD1	4	CHG_MOD2	3	CHG_MOD3
29	CHG_MOD1	4	CHG_MOD2	3	CHG_MOD3	2	
29	CHG_MOD2	3	CHG_MOD3	2		1	
29	CHG_MOD3	2		1			

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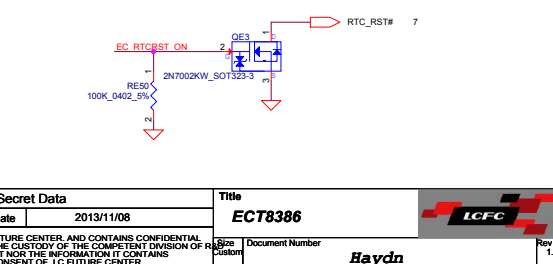
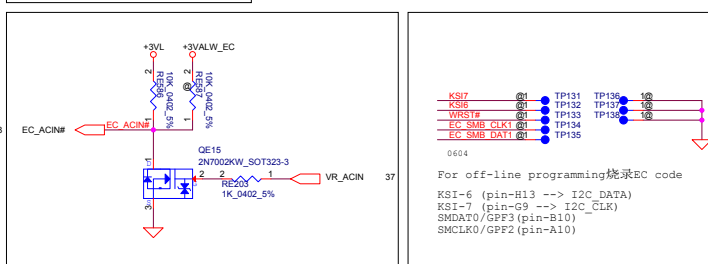
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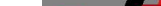
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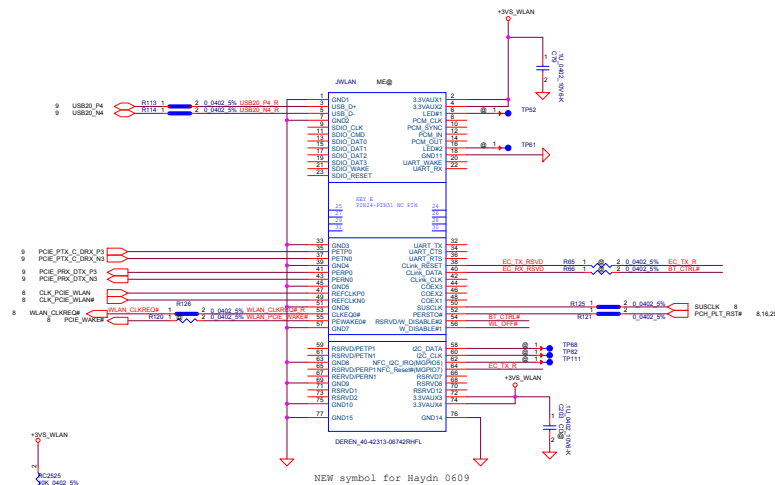
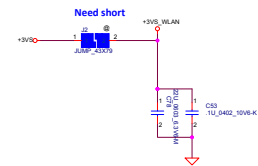
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Rev: 1.0

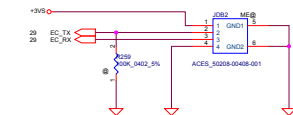
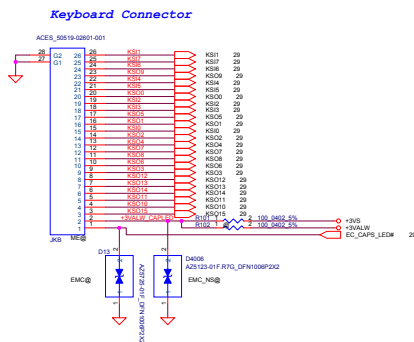
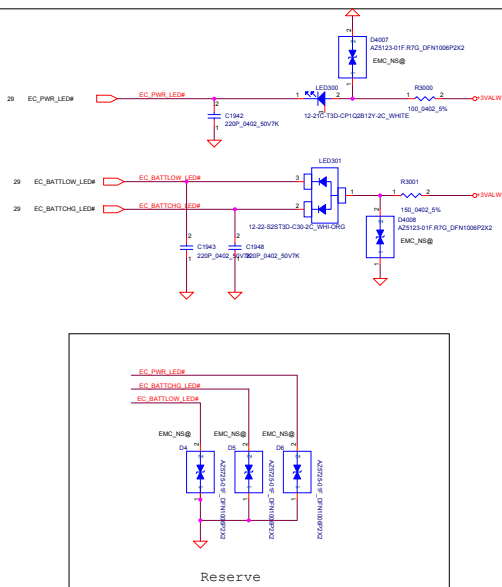
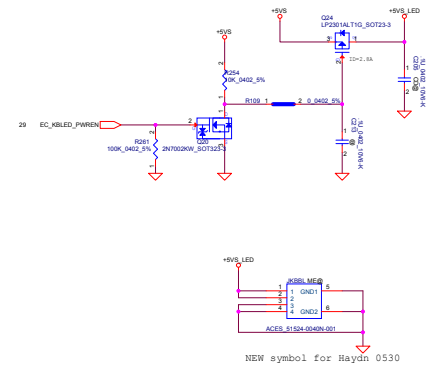
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Issued Date	2014/01/11	Deciphered Date	2013/11/08	Cardreader		
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Revision		1		Revision		1		Revision		1	



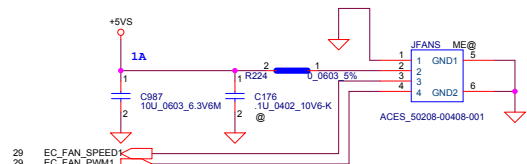
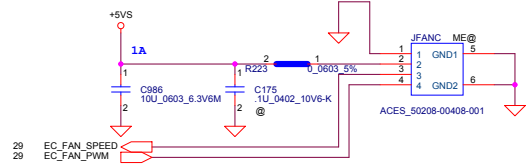
WLAN&BT Combo module circuits		
	BT on module Enable	BT on module Disable
* BT_CTRL	H	L
PCH_BT_ON#	L	H



SWAN CAS17	C117	2 EMC NSB	100 (442.500V)	EC CAS17	C133	2 EMC NSB	100 (442.500V)
K502	C83	2 EMC NSB	100 (442.500V)	K502	C83	2 EMC NSB	100 (442.500V)
K503E	C82	2 EMC NSB	100 (442.500V)	K503E	C83	2 EMC NSB	100 (442.500V)
K508	C84	2 EMC NSB	100 (442.500V)	K502	C85	2 EMC NSB	100 (442.500V)
K503E	C88	2 EMC NSB	100 (442.500V)	K502E	C87	2 EMC NSB	100 (442.500V)
K503E	C88	2 EMC NSB	100 (442.500V)	K503	C89	2 EMC NSB	100 (442.500V)
K502E	C100	2 EMC NSB	100 (442.500V)	K504E	C108	2 EMC NSB	100 (442.500V)
K501E	C118	2 EMC NSB	100 (442.500V)	K503	C120	2 EMC NSB	100 (442.500V)
K501E	C117	2 EMC NSB	100 (442.500V)	K503E	C122	2 EMC NSB	100 (442.500V)
K503E	C116	2 EMC NSB	100 (442.500V)	K505E	C108	2 EMC NSB	100 (442.500V)
K504	C115	2 EMC NSB	100 (442.500V)	K504	C123	2 EMC NSB	100 (442.500V)
K503	C121	2 EMC NSB	100 (442.500V)	K503E	C111	2 EMC NSB	100 (442.500V)
K506	C124	2 EMC NSB	100 (442.500V)	K501	C120	2 EMC NSB	100 (442.500V)

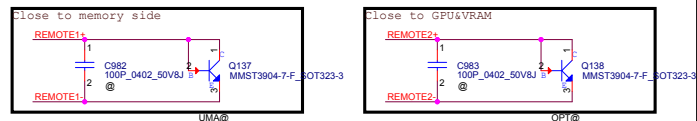
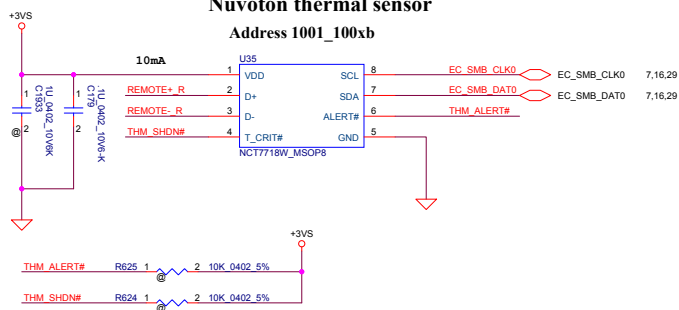
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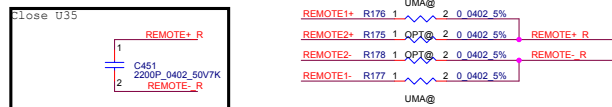


Nuvoton thermal sensor

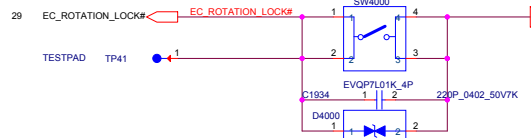
Address 1001_100xb



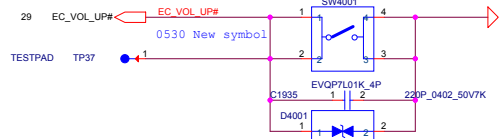
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"



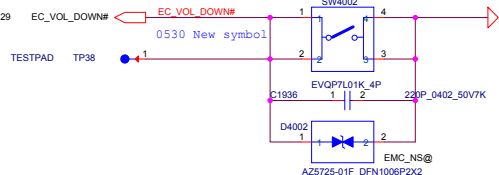
Rotation button



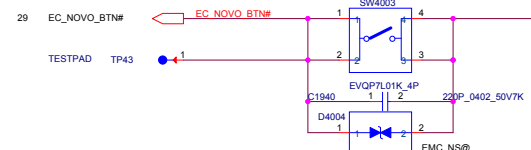
Vol up/down button



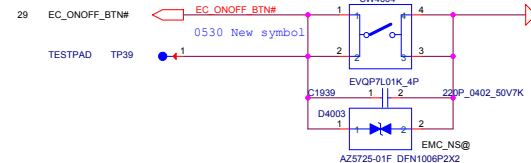
Vol up/down button



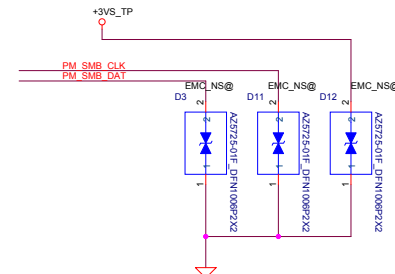
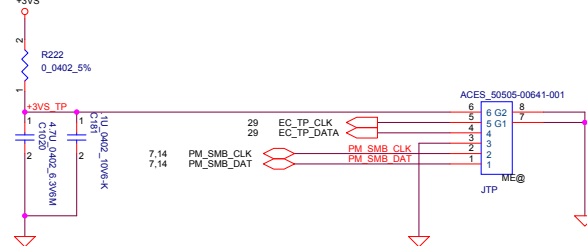
NOVO button

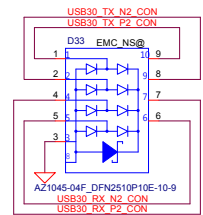
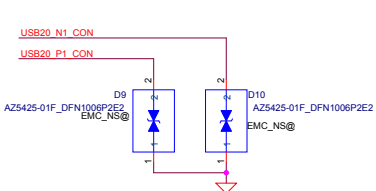
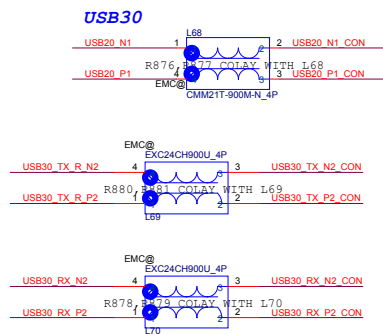


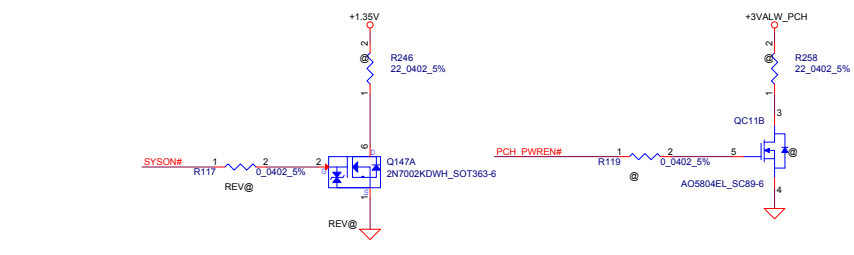
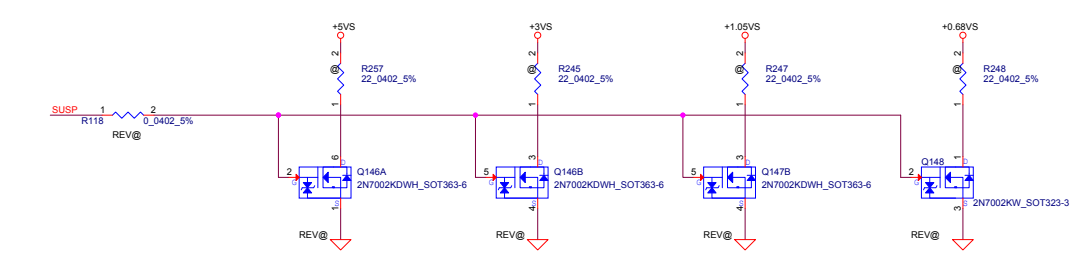
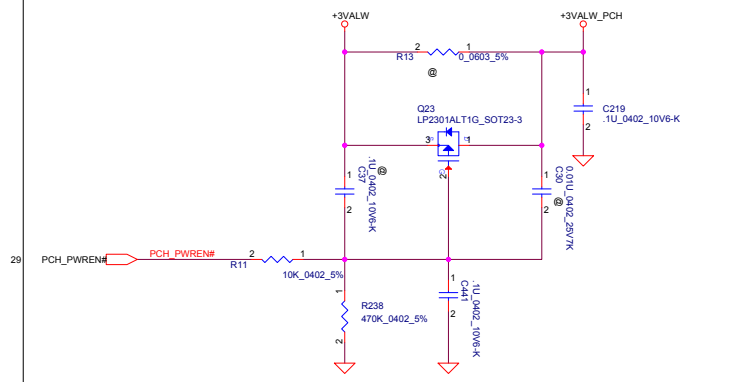
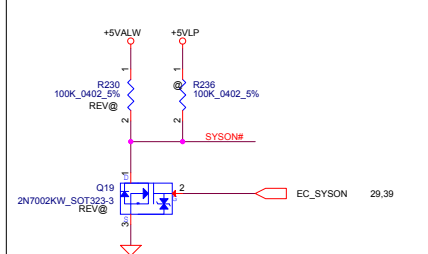
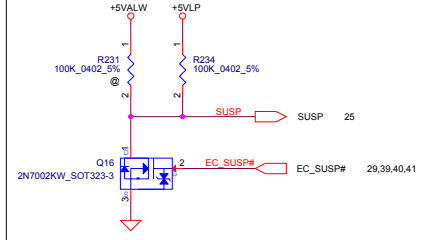
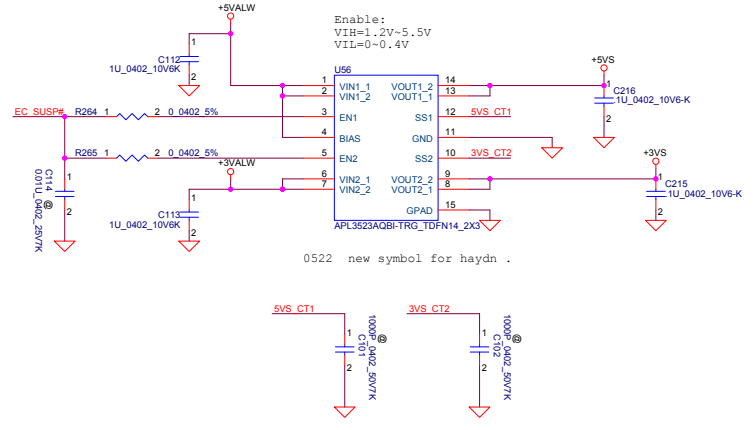
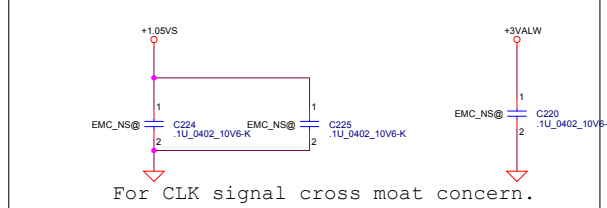
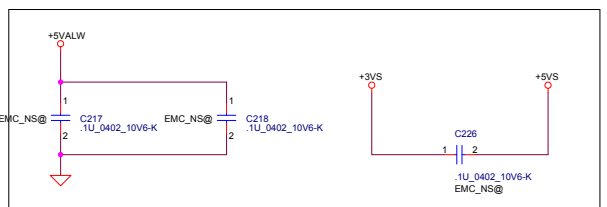
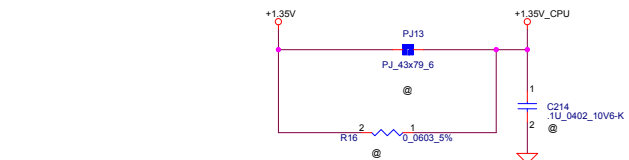
ON/OFF button



Touch Pad Connector







4/16:
1.EDP connector change to 40 pin , touch connector change to 10pin .
2.5 sensor change to BMA222E
3.Modify DIMM connector pin define

4/24:
1.CV112 change to 0.1uF follow DG.

4/28:
1.unstuff pull up pull down resistor for GPU CMD signal (Single rank no need)
2. Reserve pull down resistor for signal OVERT#
3.reserve pull up resistor for signal MULTI_STRAP_REF0_GND

4/29:
1.use buffer for signal CPU_DRAMPG_CNTL

5/4:
1.Delete N15VGM# part for Haydn only support N16S-GT.

5/6:
1.VR ADP ID change to USB ID N
2.EC ADP_ID ON# change to DCIN_USB_EN
3.Delete GPU CMD signal pull up/pull down resistor
4.update EC to LQFP package
.

5/8:
1. Change YC1,YE1 to 32.768KHZ 12.5PF_200458-PG14
2. Stuff QV7 for GPU +1.05V power
3.Add one BJT on thermal sensor for GPU&VRAM
4. Change YC1 to 32.768KHZ 12.5PF_202740-PG14

5/9:
1. modify HDMI DATA signal connection .
2. renaming GPU command signal
3.mount RC762, unmount DC27 for cost down .

5/11:
1.Change UE1 to IT8386E-192-CX LQFP128 for cost down
2.Change YC2 to 24MHZ 6PF 7V24U00032 for cost down
3.Change D4,D5,D6,D13 to ESD9N5BL-2-TR_DFN1006-2 for cost down

5/12:
1.Change JWLAN to LCN_DAN05-67146-0102
2.Delete JRTC
3.Change CC130 to SE00000P10J for cost down
4.Change D31,D32,D33 to AZ1045-04F for cost down

5/14:
1.Change R105 to 1K ohm.
2.Change CC44 to SGA00009900 for layout placement concern .
3.Change QV8,QV17,QV21 to 2N7002KDMH for layout placement concern .

5/15:
1.Change JFANC ,JFANS to 88231-04001 follow ME connector list .

5/19:
1.Touch Pad change to I2C interface.
2.Haydn support two FAN ,connect the two FAN signal to EC .
3.Delete one debug connector JDB3.
4.delete deep S3 schematic part .
5.Modify KB pin define .

5/20:
1.Move lid_pad# part schematic to USB DB .

5/21:
1.Change D34 to AZ1045-04F DFN2510P10E-10-9 follow EMC suggestion .
2.Change D7,D8,D9,D10 to AZ5425-01F follow EMC suggestion .
3.Delete SPI rom power control part schematic since not support DS3 now .
4.Touch screen part function use the same connector with EDP .

5/22:
1.Use cost down solution for signal CPU_DRAMPG_CNTL follow G .
2.Change U56 to APL3523AQBI-TRG for cost down.
3.Change JKB to ACES_50506-0260M-001 follow ME connector list .

5/26:
1.Change DV5,DV6 to BAT54AM_SOT323-3 for cost down.
2. Reserve JRTC
3. modify JLVDS pin define .
4.Delete reserved components QV24,QV25 ,DV5 for signal VGA_PWRGD

5/27:
1.Reserve CC110 for signal +1.05VS DCP5US4
2.Change JKB to ACES_50519-02601-001 follow ME connector list .
3. Change JTF to ACES_50503-0060M-001 follow ME connector list .
4. Delete WLAN AQAC part schematic .
5. Swap VRAM data group 2 ,group3 and Swap VRAM data group 6 ,group7 for layout routing concern .

5/28:
1.Reserve USB3.0 signal that connected to JIO.
2.Reserve R873,R174 for the possibility to cost down I2C redriver.
3.Change QV10,QV13 to 2N7002KDMH for layout placement concern .
4.Swap VRAM data group 4 ,group6 for layout routing concern .
5.Change RPC10 to RPC10 and RPC21 for layout concern.

5/29:
1.Reserve RV39 ,RV171 follow NVIDIA suggestion.
2.Modify JIO pin define ,add USB charger mode control signal .

0603:
1.Change JFANC ,JFANS to ACES_50208-00408-001 follow ME connector list .
2.Delete PCIE WAKE#,PCH ACIN.--reserved pull up signal +3Vt for layout concern.
3.Delete QV13",Change QV12,QV19 to 2N7002KDMH_SOT363-6 for layout concern.

0604:
1.Change JUSB30 to C-K 26211-8B19-02 follow ME connector list .
2.Change UG16 to NTSX2T02GUS XQFN8 for cost down.
3.Delete reserved component CC44 for layout concern.
4.update hole symbol.

0606:
1.Change HDMI part 0.1uF cap to 0402 size Follow DG.
2.Add reserved Caps for keyboard signal follow EMC suggestion.
3.Add reserved Caps for HDA signal follow EMC suggestion

0607:
1.Combine EC part resistor for bom quantity concern.

6/9:
1.Change JHDMI to AHRW0-AK1200 follow ME connector list .
2. Change JTF to 50505-00641-001 follow ME connector list
3.Change JIO to ACES_51540-04041-001 follow ME connector list .
4. Change JWLAN to LOTES_APCI0062-P007A follow ME connector list .

6/10:
1.Modify JLVDS pin define.
2. Add signal ILTM_SEL for USB charger.

6/12:
1.Change LV2 to PBY100505T-300Y-N ,LV1 to PBY100505T-181Y-N For smaller size.
2.Reserve RTC_RST# schematic controlled by EC.
3.Modify EC pin define(Four signals.)

6/16:
1.Change button switch SW4000,SW4001,SW4002,SW4003,SW4004 to EVQP7L01K_4P.

6/17:
1.Change QV5, QC13, QC12, QV10 to A05804EL SC89-6 for layout concern.
2.Change CV22,CC121,CC130,CC131, CV103, CVI04, CV105 to SE00000M00J for layout concern.

6/18:
1.Modify GPU power on sequence .
2.Change CV111 to SE00000M00J ,CV60 to SE107475K0J for layout concern.
3.Add thermal protection schematic .
4.Change QC11,Q149 to SB00000XFPJ for layout concern.

6/19:
1.Delete thermal protection schematic dummy components since no space to placement .

6/20:
1.Add C217,C218,C220,C224,C225,C226 For CLK signal cross moat concern .
2.Delete JCMOS1 ,add test point for signal RTC_RST#

SIV

7/21:
1.Delete CG380 For CG380/CG381 function repetition
2.Delete RV70,RV61 +1.35VGS/+1.05VGS Mosfet control signals power level change
3.Change CV54 from 0.1uf to 0.01uf. RV228 from 560ohm to 0ohm. CV506 from 0.1uf to 0.22uf for GPU power sequence change
4.Change touch pad to SMBUS solution.

7/29:
1.Delete QC5 (not connect to PCH)
2.Change RE218 from 0ohm to 100ohm for EC RSMRST# overshoot/undershot fail
3.Add CC50 0.01uf for VCCST PG_EC_R underShot fail
4.Change RC61 from 0ohm to 100ohm for SYS_PWROK overshoot/undershot fail
5.Change CC23,CC24 to 2.7pF ,CV19,CV20 to 12pF follow crystal vendor suggestion.
6.Change RE707 to 470K ,CC7 to 15pF follow crystal vendor suggestion.

08/05:
1.modify EC GPIO (EC_ON)

08/07:
1.JLVDS rotate 180 degree

08/11:
1.Change 0 ohm resistor(RC65,R184,RE188,R351,RC761,RD16,RD22, RE32, RC97, R110, R125,R121,R126
RC138,RE202,RE217,RC31,R109,R113,R114,RC758,RC759,RC105, RC103,RC99) to jump
2. NO stuff CE6 ,CD88

08/11:
1.Mount RA27 ,CA25 Follow EMC suggestion.
2. Change JIO to HRS FH52E-408-0P5SH follow ME suggestion.
3.Change JSATA to ELCO_006809610010846 follow ME suggestion.

SIT

9/23:
1.Change JLVDS to I-PEX_20374-040E-31 follow ME suggestion.
2.Change some power plane from +3VALW to +3VALW_PCH.
3.Mount D13 follow emc suggestion.


9/24:
1.Reserve CC31 and CC32 For EMC.

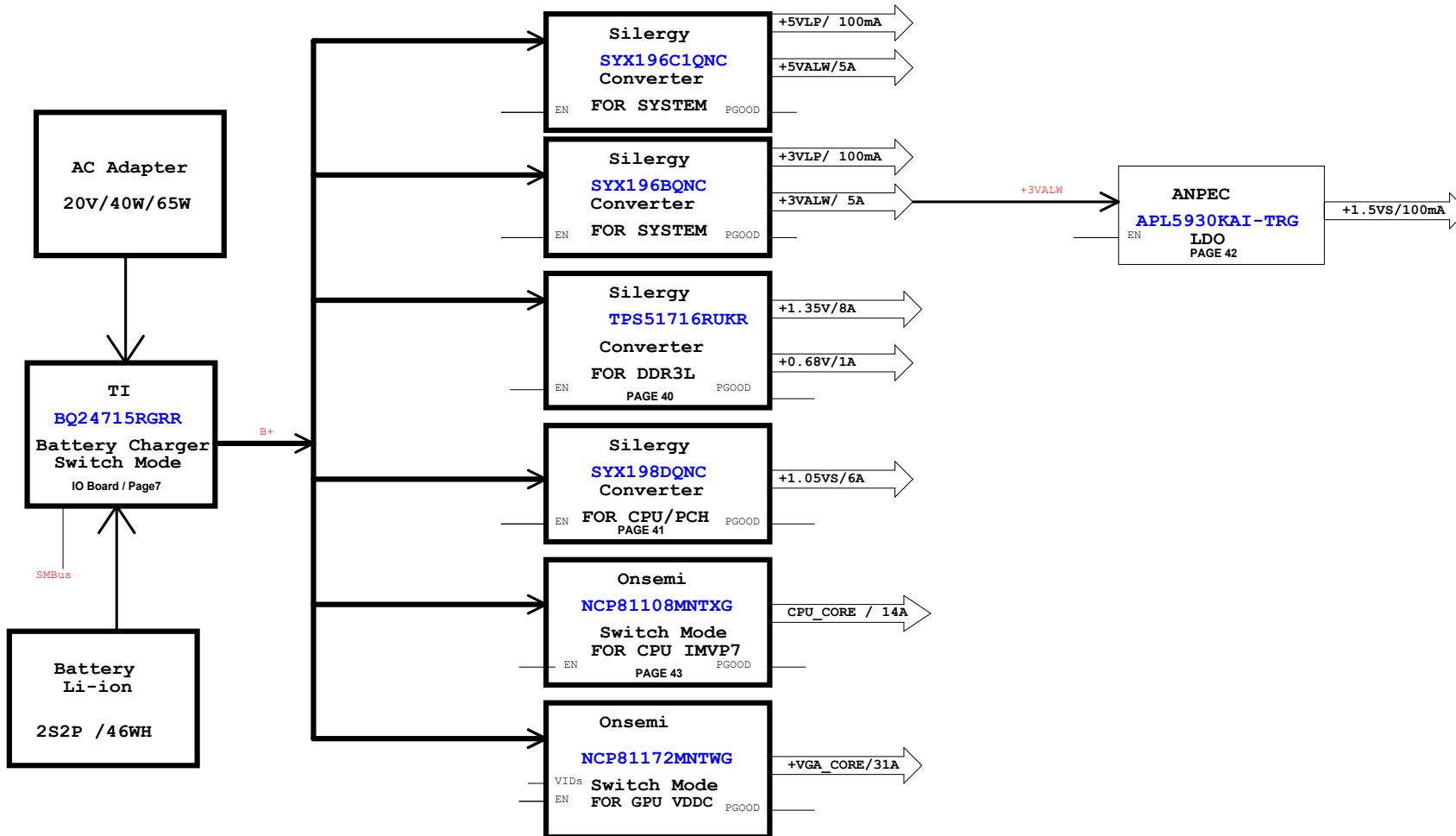
9/25:
1.Mount RE254 ,CE339 For EMC.
2.Change RE22 , RE23 ,RC62 ,RC81 ,RC85 ,R909 ,R223,R224 to R short.
3.Change L69,L70 to EXC24CH900U for cost down

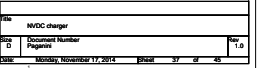
10/13:
1.Change CC23,CC24 to 3.3pF for RTC Time test fail in windows.

11/11:
1.Change CE339 to 18pF for HSW platform LPC CLK fall slew rate test fail issue.

11/13:
1.Change R2,R22,R5,R13,RG20,R26,RC107,RC122,RC124,RE214,RE215,RE216 to R short for cost down.
2. Mount RE50,QE3,Q23,R11,R238,C441 for clear CMOS.
3.Change JWLAN to DEREN_40-42313-06742RHFL follow ME request.
4.Change JUSB30 to DEREN_40-42039-00901RHF-L Follow ME request.

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Issued Date		2014/01/11		Deciphered Date		2013/11/08				HW_Change_List	
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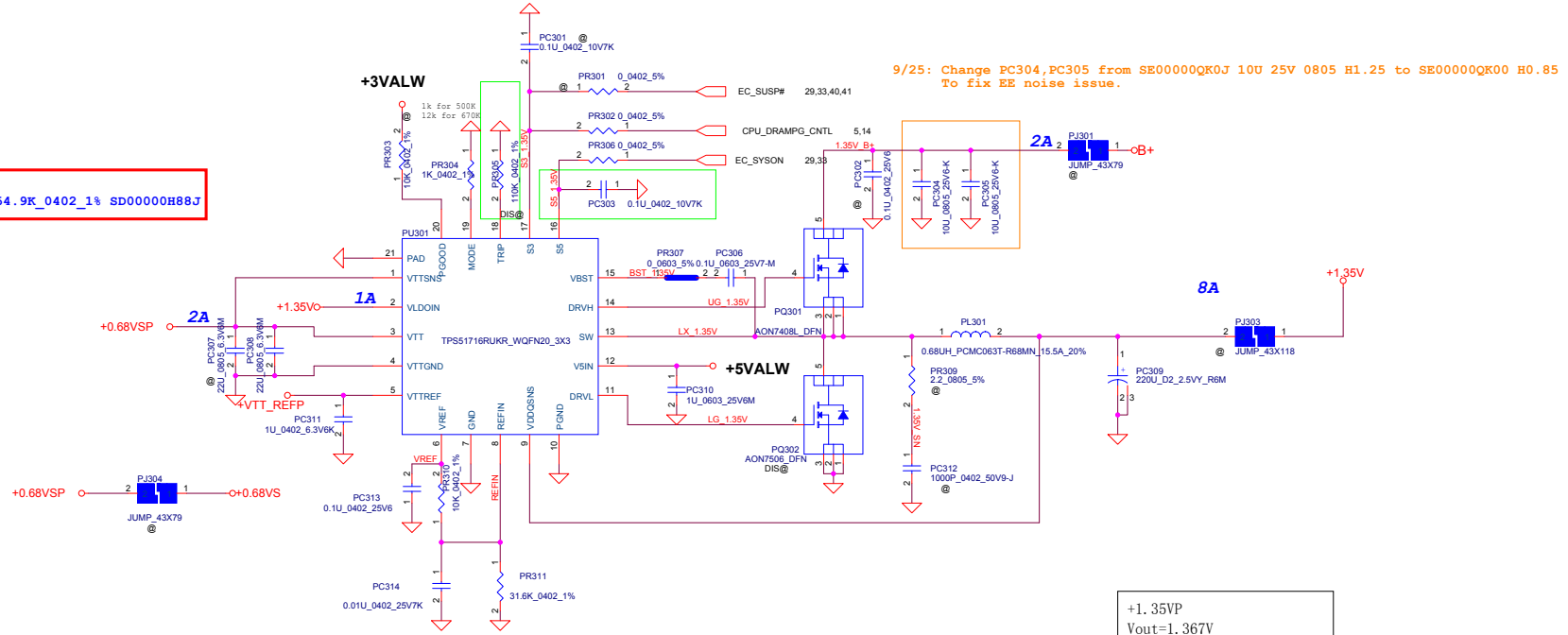
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VFB=2V	TDC 5A
TDC 5A	
Fsw=350KHZ	Fsw=300KHZ
OCF:7.8A~9.5A	OCF:7.8A~9.5A

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8/1: Follow EE request to stuff PC303 0.1u_0402_10v7k for EC_SYSON overshoot/undershot fail

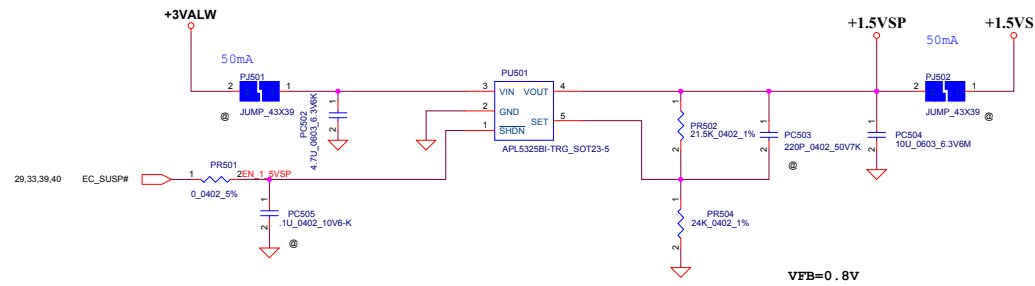
9/25: Change PC304,PC305 from SE000000QK0J 10U 25V 0805 H1.25 to SE000000QK00 H0.85 To fix EE noise issue.

UMA SKU OCP
PR305 change to 54.9K_0402_1% SD00000H88J

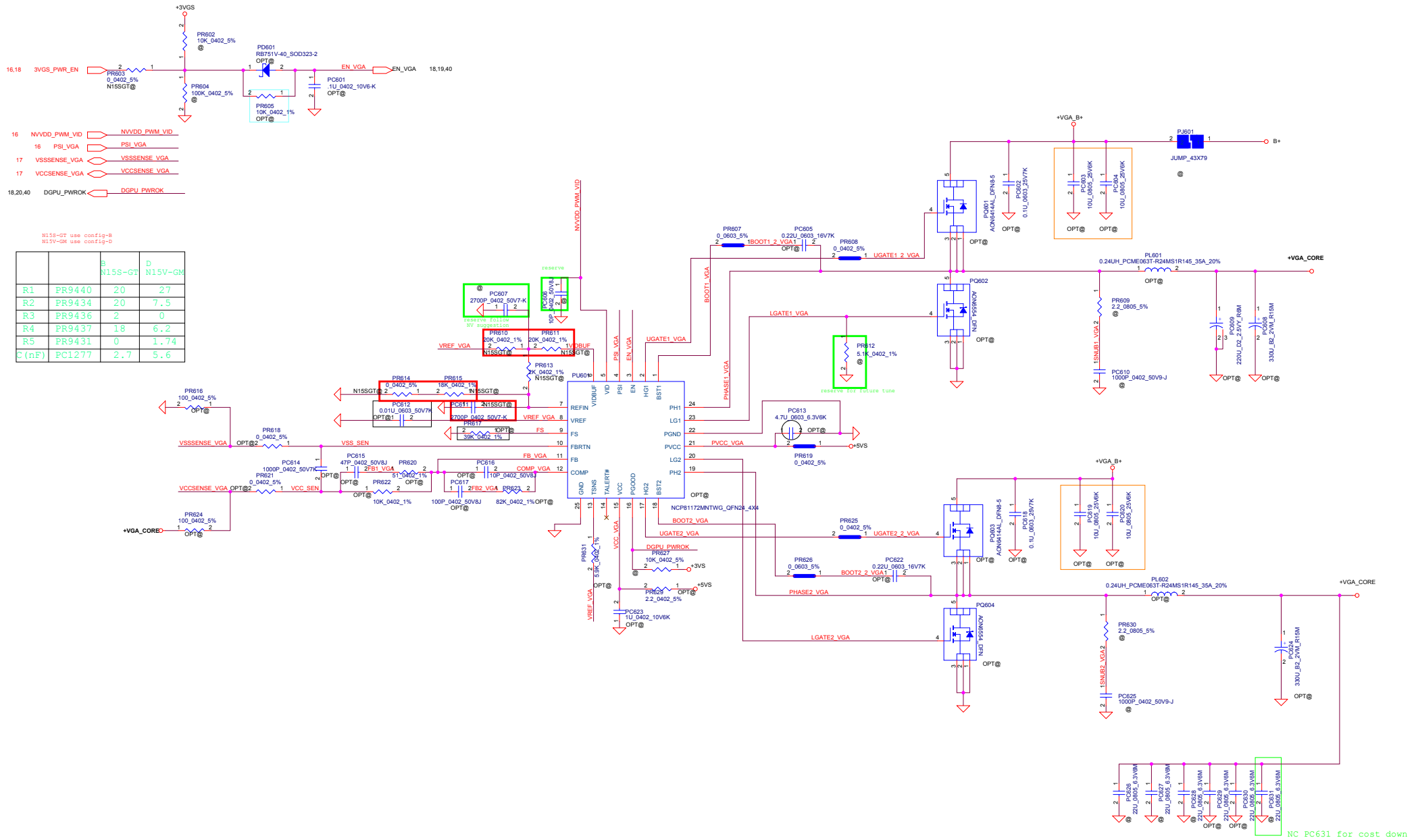



UMA SKU
PQ302 change to AON7408L for 4A output current

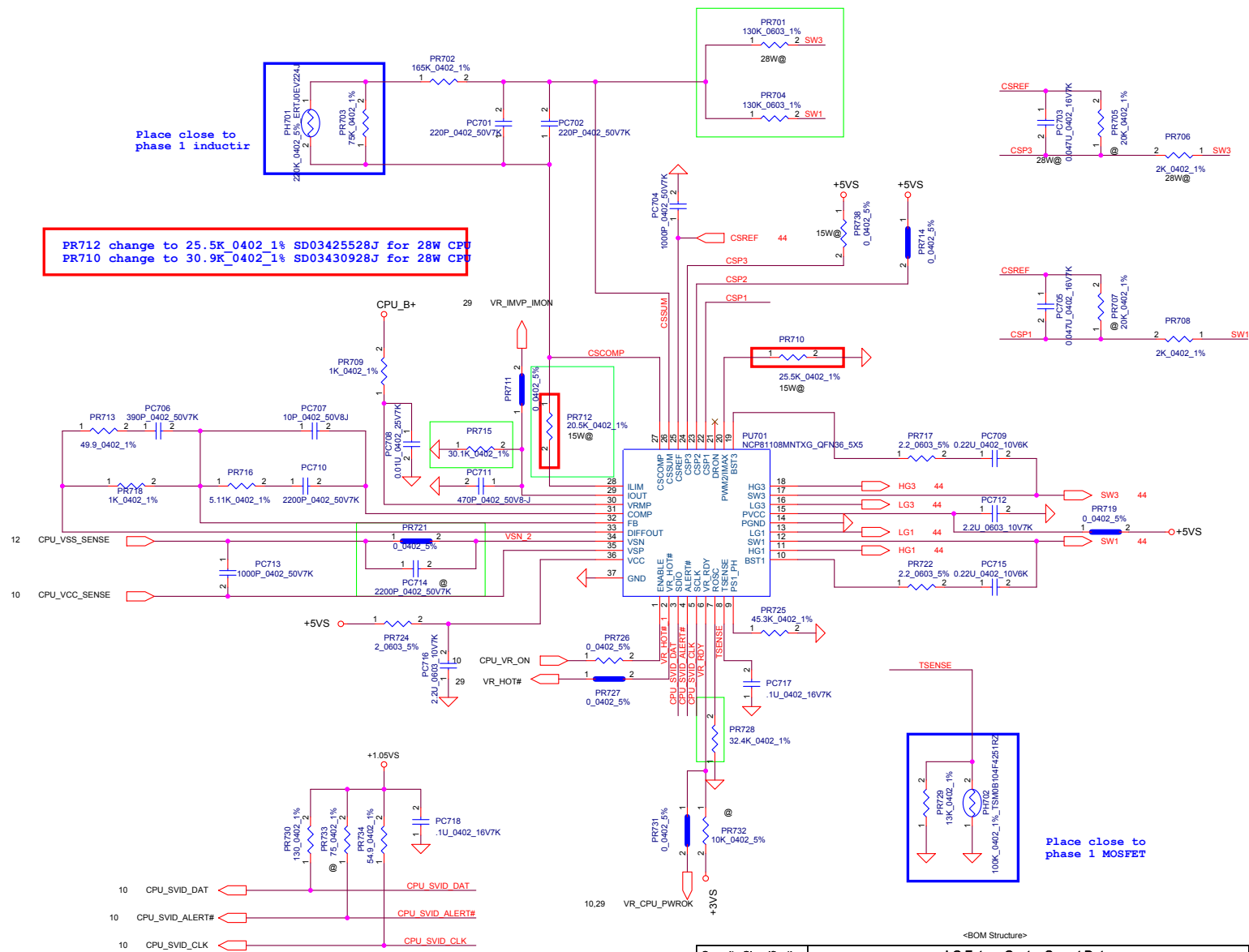
+1.35VP
Vout=1.367V
Iocp min=13A fro DIS SKU
Iocp min=6A fro UMA SKU



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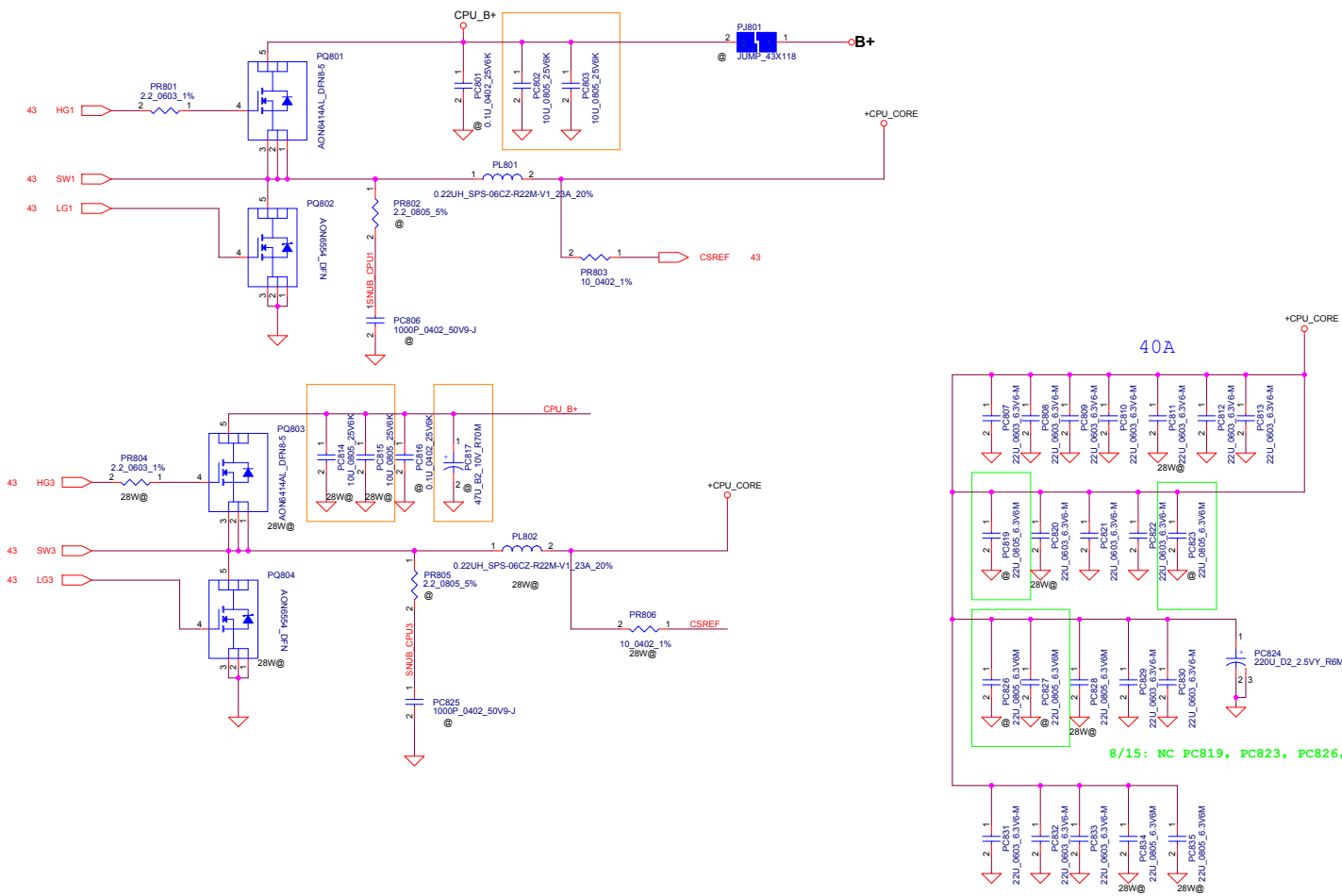
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8/15: NC PC819, PC823, PC826, PC827 for cost down.

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